TIME BASE GENERATOR INTERFACE KIT

OPERATING AND SERVICE MANUAL 20 AUG 1968

SECTION I

INTRODUCTION AND DESCRIPTION

1-1. INTRODUCTION.

1-2. Interface Kit 12539A generates real time intervals in decade steps from 100 microseconds to 1000 seconds (16.67 minutes) derived from a crystal oscillator. This card can be used as a source of timed interrupt for software clock. The kit consists of the following:

a. Interface Kit 12539A Time Base Generator Card, HP Part No. 02116-6119.

b. Time Base Generator Test.

1-3. Sections II through IV provide installation and programming, theory of operation and replaceable parts information for the Time Base Generator Card. Section V contains troubleshooting information. A supplement to this manual contains a description of the diagnostic program contained on the Time Base Generator Test-Binary Tape and the diagnostic listing.

1-4. DESCRIPTION.

1-5. The Time Base Generator Card contains command and interrupt logic, a 100 kHz oscillator, and eight decade frequency dividers. This card plugs into any of the interface card I/O slots of the Computer and assumes the lower Select Code of the slot.

1-6. <u>SPECIFICATIONS</u>.

Stability: 2 parts in 10^6 per week.

Temperature Effects: 20 parts in 10^6 over the temperature range of 15 to 35 C.

Total Stability: 1/2 second per 24-hour day.

SECTION II

INSTALLATION AND PROGRAMMING

2-1. INSTALLATION.

2-2. Open the Computer for access to the I/O cards and insert the Time Base Generator card in the desired I/O slot of the Computer. The slot connector transfers all signals to and from the Computer; no additional cabling is required. Close the Computer.

2-3. PROGRAMMING.

2-4. Table 2-1 provides a typical program example. This example is a subroutine which provides an execution delay of 8 milliseconds using the Time Base Generator. The "flag-test" (SFS) method is used, rather than interrupt.

Table 2-1. Program Example

```
DELAY    NOP
         LDA      .8         GET 8 FOR COUNTER
         CMA,     INA        MAKE NEGATIVE
         STA      COUNT      INITIALIZE COUNTER
         LDA      .1         GET CONTROL WORD FOR
         OTA      TBG        1 MILLISEC FLAGS & OUTPUT
LOOP     STC      TBG,C      START TIME BASE GEN.
         SFS      TBG        HAS PERIOD ELAPSED
         JMP      *-1        NO – CONTINUE TO WAIT
         ISZ      COUNT      1 PERIOD HAS ELAPSED
         JMP      LOOP       NOT THE LAST ONE, START ANOTHER
         JMP      DELAY,I    TOTAL DELAY HAS ELAPSED, RETURN
*
TBG      EQU      nn         I/O ADDRESS OF TIME BASE GEN.
COUNT    NOP                 LOCATION OF FLAG COUNTER
.8       DEC      8          FOR 8 FLAGS
.1       OCT      1          CONTROL WORD FOR 1 MILLISEC
```


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THEORY OF OPERATION

3-1. GENERAL THEORY OF OPERATION.

3-2. An Output from A (OTA) or an Output from B (OTB) instruction applies a 3-bit binary number to the Time Base Selection flip-flops, Bit 0, Bit 1, and Bit 2. This 3-bit number (IOBO0, IOBO1, and IOBO2) determines the time interval between interrupt (or SKF) signals to the Computer and are the three least significant bits of the A- or B-Register. When a different time interval is desired, the 3-bit number is changed (with another OTA/B instruction). For non-decade time intervals (e.g., 3 milliseconds), the nearest decade interrupt must be counted in software to form the desired interval. Table 3-1 lists the Computer outputs and the respective time intervals available from the card. Note that interrupt (or SKF) signals can be programmed to occur every 10^{n-1} milliseconds, where n is the 3-bit binary number from the A- or B-Register.

Table 3-1. Time Intervals

I/O BUS OUTPUT (IOBO)			TIME INTERVAL
Bit 2	Bit 1	Bit 0	
0	0	0	0.1 Millisecond
0	0	1	1 Millisecond
0	1	0	10 Milliseconds
0	1	1	0.1 Second
1	0	0	1 Second
1	0	1	10 Seconds
1	1	0	100 Seconds
1	1	1	1000 Seconds

3-3. As a result of the OTA/B instruction, the IOO signal causes the Time Base Selection flip-flops and the eight decade dividers to be reset at time T3 to establish proper initial conditions. The IOBO signals cause the Time Base Selection flip-flops to set or remain reset, as applicable, and the flip-flop outputs provide enabling signals to the "and" gates on the outputs of the decade dividers. At this time, the output of the 100 kHz Oscillator is not enabled to the decade dividers since the Control flip-flop is still in a reset state.

3-4. A Set Control, Clear Flag (STC,CLF) instruction to the Time Base Generator Card initiates the time interval programmed by the OTA/B instruction. The STC portion of the instruction sets the Control flip-flop, which enables the Oscillator output to the decade dividers and resets the Error flip-flop. The Error flip-flop is set if the interrupt signal at the end of the programmed time interval is not acknowledged. The CLF portion of the instruction resets the Flag flip-flop so that it can be set to indicate the end of the selected time interval using the SFS instruction.

3-5. DETAILED THEORY OF OPERATION.

3-6. Figure 3-1 depicts the logic diagram for the Time Base Generator Card and Figure 3-2 depicts the location of parts on the board. Logic diagram reference designations preceded by MC are identified by part number in Section IV and the logic diagram for each Microcircuit package is shown in Figure 3-3.

3-7. TIME BASE SELECTION.

3-8. The outputs of the decade dividers are "anded" with the outputs of the Time Base Selection flip-flops. The output of the particular enabled "and" gate is combined with the true output of the Control flip-flops, and the true reset output of the Flag flip-flop to provide a true output from "and" gate MC87C. The output of MC87C is applied to the Flag Buffer flip-flop. The Flag Buffer flip-flop will not set until its input signal drops. This occurs when the applicable decade divider square-wave output drops, causing the output of gate MC87C to become false. After the Flag Buffer flip-flop is set, the Flag flip-flop sets on the arrival of the ENF signal at time T2 of the machine cycle. The interrupt or SKF signal (as applicable) is then initiated to the Computer, indicating the end of the selected time interval. (If the SKF method is to be used, a Skip on Flag Set (SFS) or a Skip on Flag Clear (SFC) instruction must be issued to test the condition of the Flag flip-flop.)

3-9. Assume a 3-bit (IOBO) input to the Time Base Selection flip-flops of 000. The true reset outputs of the flip-flops are applied to "and" gate MC45B. All other "and" gates contain at least one false input from the Time Base Selection flip-flops. When a STC instruction is issued, the Oscillator output is enabled to decade divider MC93. The square-wave output of MC93 becomes true and then returns to a false condition 0.1 millisecond after the STC instruction is issued. During the 0.1 millisecond interval, a true signal is applied to the Flag Buffer flip-flop. At the end of the interval, the Flag Buffer flip-flop sets and the interrupt and SKF circuits are initiated.

3-10. ERROR DETECTION.

3-11. The output of the particular enabled "and" gate on the output of the decade divider is combined with the set output of the Flag flip-flop at "and" gate MC123A. Therefore, the Error flip-flop is set if the Flag flip-flop is set. The Flag flip-flop will be set during the present time interval only when the previous time interval was not acknowledged by the Computer. (A Clear Flag (CLF) instruction must be issued after each time interval to permit recognition of the following time interval.) The condition of the Error flip-flop can be tested by a Load Into A (LIA) or a Load Into B (LIB) instruction. The IOI signal resulting from the LIA or LIB instruction enables "and" gate MC107A to provide a true IOBI4 signal to the A- or B-Register of the Computer. Therefore, if bit 4 of the applicable Register is true, at least one time interval was missed. The Error flip-flop is reset again by a CLF, STC instruction.

3-12. At completion of the use of the Time Base Generator card, a Clear Control (CLC) instruction should be programmed to reset the Control flip-flop and all decade dividers.

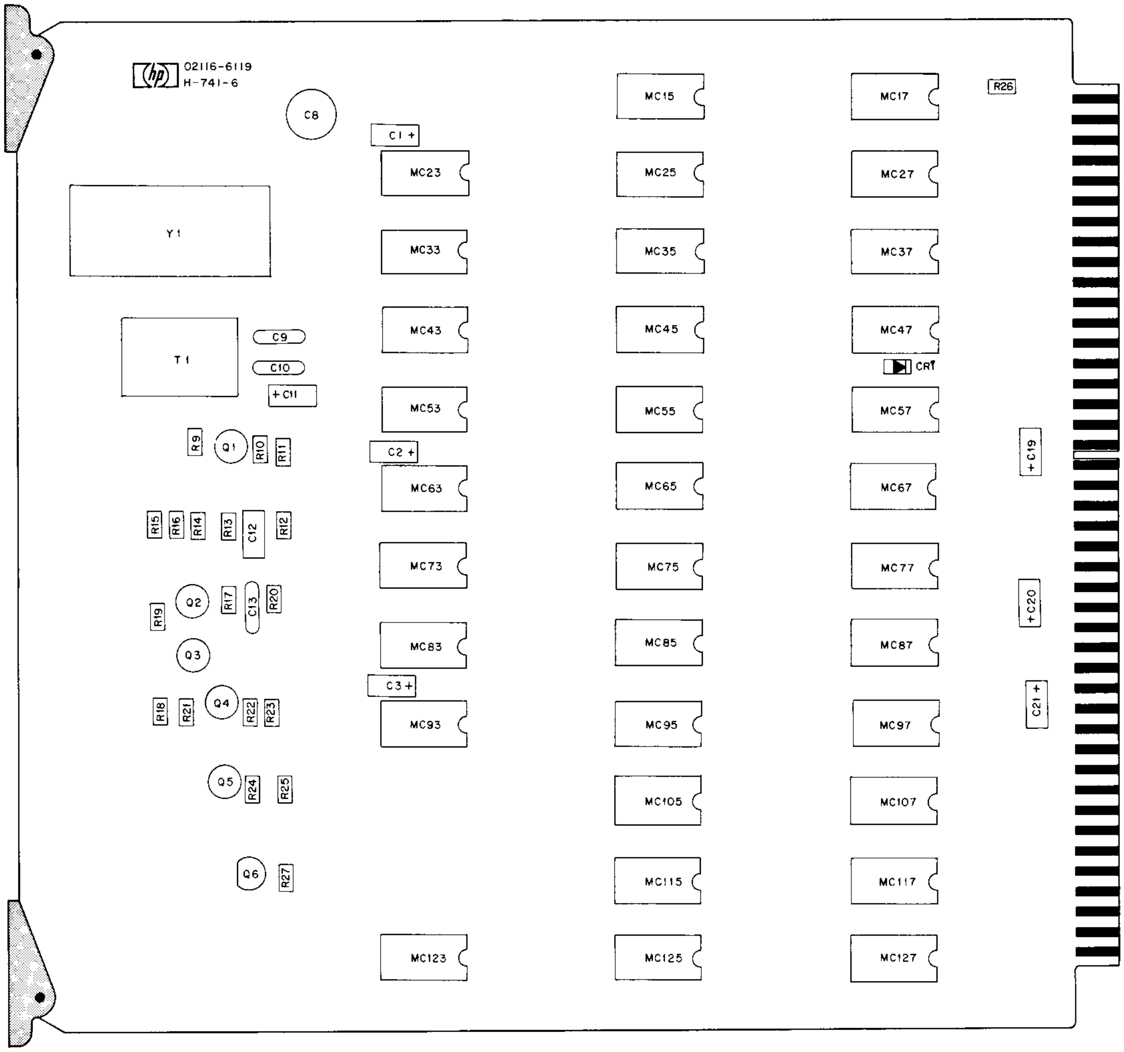

Figure 3-2. Time Base Generator, Parts Location Diagram

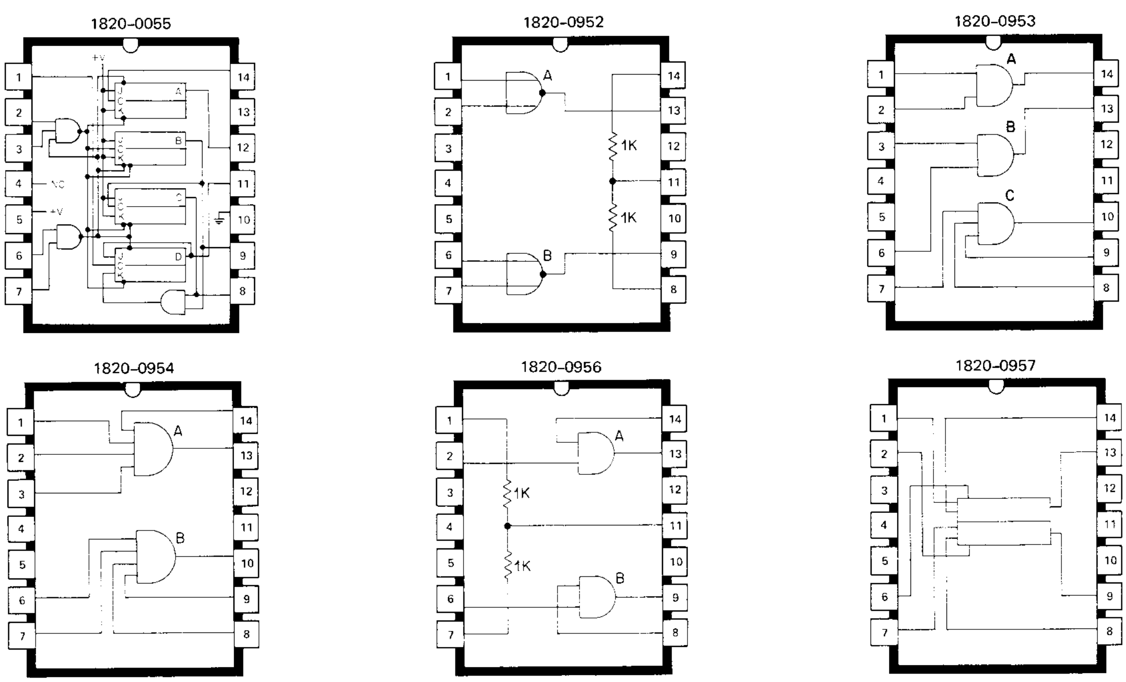

Figure 3-3. Microcircuit Packages, Top View

SECTION IV

REPLACEABLE PARTS

4-1. INTRODUCTION.

4-2. This section contains information for ordering replacement parts for the Time Base Generator Card. Refer to Table 4-1 for a list of replaceable parts in alpha-numerical order of their reference designations, with a description and HP part number for each part.

4-3. ORDERING INFORMATION.

4-4. To order a replacement part, address the order or inquiry to your local Hewlett-Packard field office. See the list at the back of this manual for field office addresses.

4-5. Specify the following information for each part when ordering:

a. Hewlett-Packard part number
b. Circuit reference designation
c. Description

4-6. To order a part not listed in Table 4-1, give a complete description of the part and include its function and location.

Table 4-1. Replaceable Parts for Time Base Generator Card

REFERENCE DESIGNATION	DESCRIPTION	HP PART NO.	MFR CODE	MFR PART NO.
C1,2,3,11,19,20,21	Capacitor, fixed, Tant, 1.0 uf ±10%	0180-0291	56289	150D105X9035A2
C8	Capacitor, variable, 9 to 35 pf	0121-0046	72982	538-011-E2PO-94R
C9 Factory	Capacitor, fixed, mica, 27 pf ±5%	0160-2101	72136	RDM15E270G3C
C9 adjusted	Capacitor, fixed, mica, 24 pf ±5%	0160-0196	04062	RDM15C240J3S
C9 value	Capacitor, fixed, mica, 20 pf ±5%	0140-0204	72136	RDM15C200J3C
C10	Capacitor, fixed, mica, 470 pf ±5%	0140-0149	72136	DM15F471J
C12	Capacitor, fixed, Mylar, 0.001 uf ±10%	0160-0153	56289	192P10292-PTS
C13	Capacitor, fixed, mica, 220 pf ±5%	0160-0134	72136	DM15F221J (300V)
CR1	Diode	1910-0022	28480	-
MC15,25,35,45,97	Integrated Circuit	1820-0954	28480	-
MC17,107	Integrated Circuit	1820-0956	28480	-
MC23,33,43,53,63,73,83,93	Integrated Circuit	1820-0055	28480	-
MC27,57,65,75,85,95,115,127	Integrated Circuit	1820-0952	28480	-
MC37,47,55,77,87,105,117,123,125	Integrated Circuit	1820-0953	28480	-
MC67	Integrated Circuit	1820-0957	28480	-
Q1	Transistor, Silicon, NPN (S6515)	1854-0019	28480	-
Q2 thru Q5	Transistor, Silicon, NPN (2N3646)	1854-0094	28480	-
Q6	Transistor, Silicon, PNP (2N3906)	1853-0036	28480	-
R9	Resistor, fixed, 68K ±5%, 1/4W	0683-6835	01121	CB 6835
R10,20	Resistor, fixed, 10K ±5%, 1/4W	0683-1035	01121	CB 1035
R11	Resistor, fixed, 47 ohms ±5%, 1/4W	0683-4705	01121	CB 4705
R12	Resistor, fixed, 8.2K ±5%, 1/4W	0683-8225	01121	CB 8225
R13	Resistor, fixed, 2.2K ±5%, 1/4W	0683-2225	01121	CB 2225
R14	Resistor, fixed, 33K ±5%, 1/4W	0683-3335	01121	CB 3335
R15	Resistor, fixed, 3.9K ±5%, 1/4W	0683-3925	01121	CB 3925
R16	Resistor, fixed, 2.7K ±5%, 1/4W	0683-2725	01121	CB 2725
R17	Resistor, fixed, 150 ohms ±5%, 1/4W	0683-1515	01121	CB 1515
R18	Resistor, fixed, 1.8K ±5%, 1/4W	0683-1825	01121	CB 1825
R19,21	Resistor, fixed, 6.8K ±5%, 1/4W	0683-6825	01121	CB 6825
R22	Resistor, fixed, 4.7K ±5%, 1/4W	0683-4725	01121	CB 4725
R23,25,26	Resistor, fixed, 470 ohms ±5%, 1/4W	0683-4715	01121	CB 4715
R24,27	Resistor, fixed, 1K ±5%, 1/4W	0683-1025	01121	CB 1025
T1	Transformer	5212A-9A	28480	-
Y1	Crystal Oscillator, 100 kHz	0410-0021	28480	-

SECTION V

TROUBLESHOOTING

5-1. DIAGNOSTIC TEST.

5-2. To confirm proper operation of the Time Base Generator option, use the Diagnostic Test tape furnished with the Interface Kit. The operating procedure and all pertinent information, including the program listing, is supplied in the Time Base Generator Diagnostic Test supplement (a supplement to this manual).

5-3. If the Diagnostic indicates a failure of the Time Base Generator, the following procedures may be used to check the basic timing signals.

5-4. OSCILLATOR TEST.

5-5. Testing of the 100 kHz Oscillator on the Time Base Generator Card is accomplished with the card plugged into a single connector extender which is plugged into the Computer. Turn Computer power on. The output of the oscillator is checked at test point TP1, Figure 3-1. If the oscillator is operating properly, a 100 kHz non-symmetrical square-wave should be observed. The same square-wave should be observed at test point TP2 after the Control flip-flop is set by an STC instruction.

5-6. Replacement of crystal Y1, capacitors C8 or C9 may require selection of C9 to give proper circuit operation. Adjustment of C8 should allow tuning 100 kHz ±0.5 Hz. The value of C9 should be as large as possible while tuning this range. If the value of C9 is small and the value of C8 is large, the temperature stability is poorer.

5-7. The negative portion of the waveshape (between R13 and C12) should be flattened. This indicates sufficient loop gain to saturate while rotating C8 through its entire range. This ensures enough loop gain to oscillate at low temperature. A frequency standard of adequate accuracy should be used for selecting C9 (accuracy $1/10^7$, readout 7 significant digits).

5-8. DECADE DIVIDER TEST.

5-9. To facilitate testing of the eight decade dividers (MC23, MC33, MC43, MC53, MC63, MC73, MC83, and MC93), the Time Base Generator Card is designed to accept a jumper (W2) between the output of MC93 and the input to MC53. With this jumper installed use an oscilloscope for testing. Before testing the decade dividers, the W2 jumper may be installed to cause reduction of the time interval for the last group of four decade dividers to one second. To enable the 100 kHz Oscillator output to the dividers, the Control flip-flop must be set by an STC instruction. At completion of testing, the W2 jumper must be removed if the card is to function properly.