7254
QUAD VMOS DRIVE TRANSISTORS FOR BUBBLE MEMORIES

- **Designed to Drive X and Y Coils of 7110 Bubble Memories**
- **No Bias Currents Required**
- **Fast Turn-On and Turn-Off: 30 ns Maximum**
- **Built-In Diode Commutates Coil Current When Transistor is Turned Off**
- **Operates from V_{DD} Only**
- **VMOS FET Technology**
- **N-Channel and P-Channel Transistors in the Same Package**
- **Standard 14-Pin Dual-In-Line Package**

The 7254 is a quad transistor pack designed to drive the X and Y coils of Intel Magnetics Bubble Memories. Two 7254 packages are required for each bubble memory device. Each 7254 package would drive either the X or Y coil as shown under "circuit diagram." This recommended connection circuit takes into account the fact the Q1/Q2 and Q3/Q4 are tested as a pair for "On" resistance value to assure optimal bubble performance.

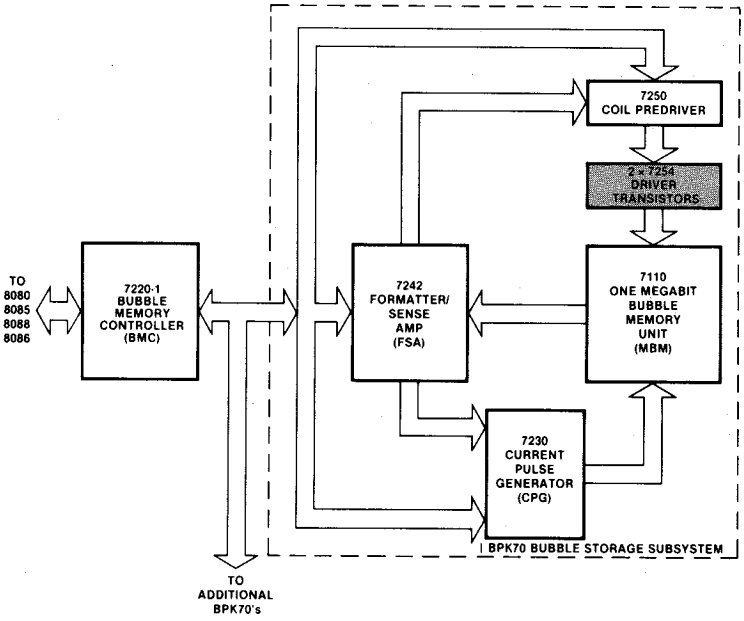

Figure 1. Block Diagram of Single Bubble Memory System—128K Bytes

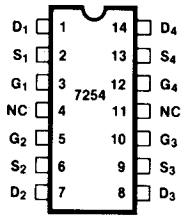

Figure 2. Pin Configuration

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ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ... −40°C to +100°C
Storage Temperature ..... −65°C to +150°C
Gate Voltage (with respect to
Source and Drain 15V
Continuous Drain Current 2A
Peak Drain Current 3A
Power Dissipation (T_A = 80°C) 1.05W
Power Dissipation (T_A = 25°C) 1.75W

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS All Limits Apply for N- and P-Channel transistors, T_A = −30° to 85°C unless otherwide noted.

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Unit	
BV_{DSS}	Drain-Source Breakdown Voltage	20			V	V_{GS} = 0, I_D = 10 μA
$V_{GS}(th)$	Gate-Source Threshold Voltage	0.8			V	V_{GS} = V_{DS}, I_D = 1 mA, T_A = 25°C
		0.65			V	V_{GS} = V_{DS}, I_D = 1 mA, T_A = 85°C
I_{GSS}	Gate Leakage Current			100	nA	V_{GS} = 12V, V_{DS} = 0, T_A = 25°C
I_{DSS}	Drain Leakage Current			500	nA	V_{GS} = 0, V_{DS} = 20V, T_A = 25°C
R_{DS}	On-Resistance for sum of Q1+Q2, Q3+Q4 (Note 1)	2.0	2.5	3.0	Ω	V_{GS} = 11.4V, 1_D = 1A, T_A = 25°C
V_{F1}	Parasitic Diode Forward Voltage (Note 1)			.75	V	V_{GS} = 0V, I_D = 50 mA, T_A = 25°C
V_{F2}	Parasitic Diode Forward Voltage (Note 1)			1.20	V	V_{GS} = 0V, I_D = 1000 mA, T_A = 25°C

NOTE:
1. Pulse test—80 μs pulse, 1% duty cycle, r_{DS} increase 0.8%/°C.

A.C. CHARACTERISTICS T_A = 25°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$T_{ON}(N)$	N-Channel Turn-On Time			20	ns	
$t_{ON}(P)$	P-Channel Turn-On Time			30	ns	
$t_{OFF}(N)$	N-Channel Turn-Off Time			20	ns	
$t_{OFF}(P)$	P-Channel Turn-Off Time			30	ns	

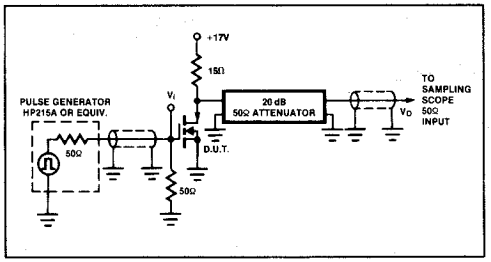

Figure 3. Switching Time Test Circuit

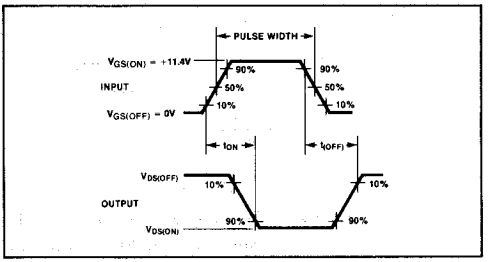

Figure 4. Switching Time Test Waveforms

CAPACITANCE $T_A = 25°C$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$C_{iss}(N)$	N-Channel Input Capacitance			175	pF	$V_{GS} = 0$, $V_{DS} = 12V$, f = 1 MHz
$C_{iss}(P)$	P-Channel Input Capacitance			190	pF	$V_{GS} = 0$, $V_{DS} = 12V$, f = 1 MHz

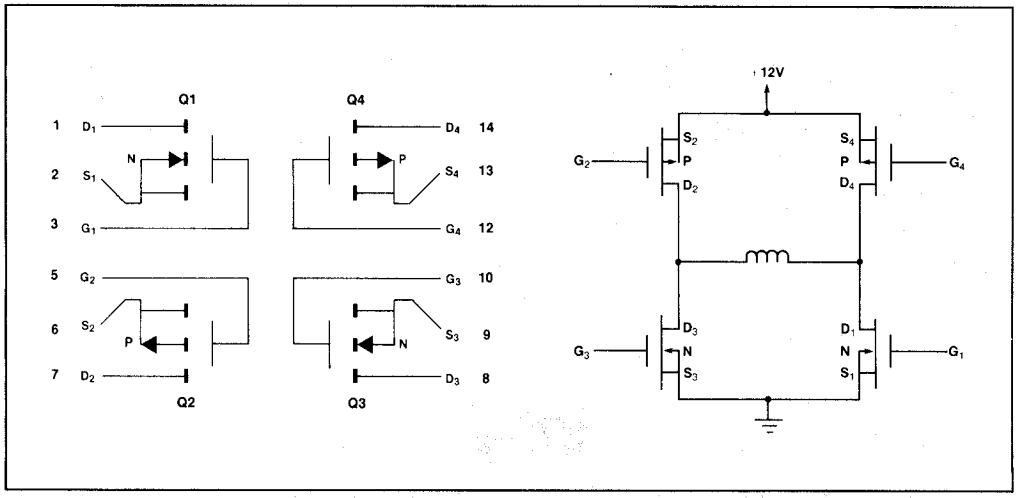

Figure 5. Circuit Diagram

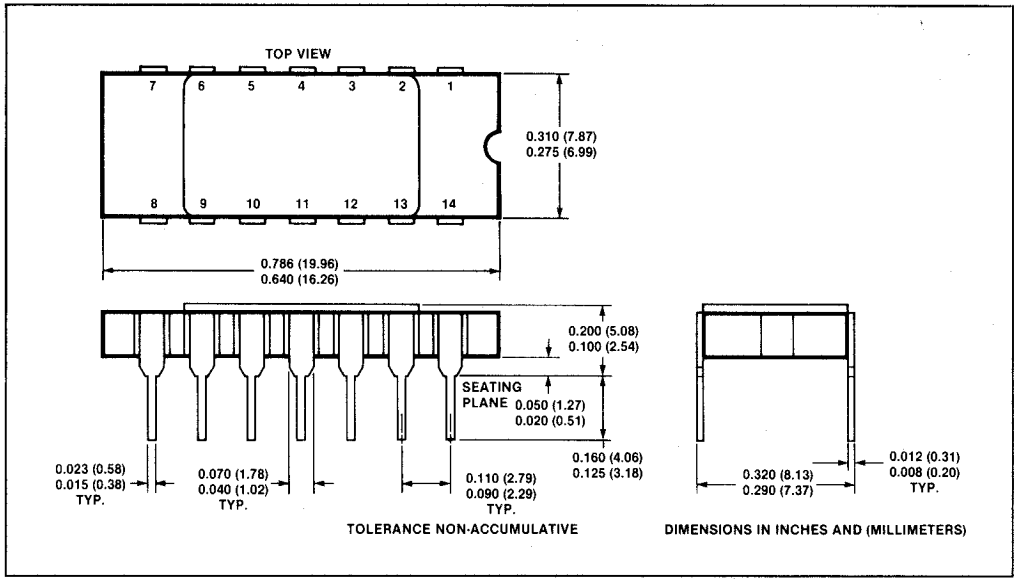

Figure 6. Packaging Information

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INTEL CORPORATION, 3065 Bowers Avenue, Santa Clara, CA 95051 (408) 987-8080

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