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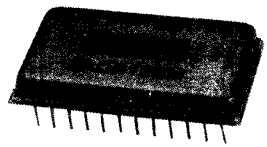
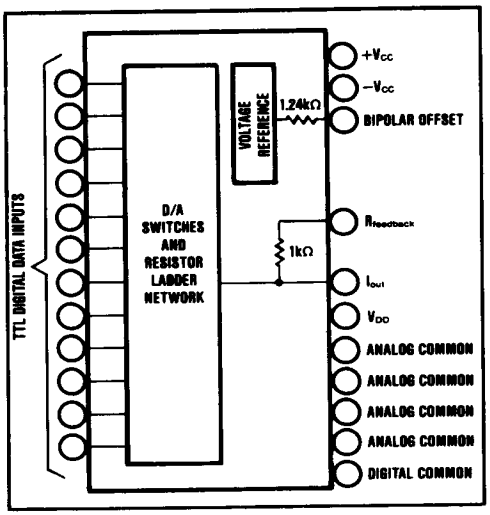


DAC812

Ultra-High Speed DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 12-BIT RESOLUTION AND ACCURACY
- 55nsec CURRENT OUTPUT SETTLING TIME
- TTL-COMPATIBLE INPUTS
- MONOTONIC OVER ENTIRE TEMPERATURE RANGE
- LINEARITY ERROR LESS THAN ±1/2LSB OVER TEMPERATURE RANGE (C GRADE)
- HERMETIC METAL PACKAGE



DESCRIPTION

The DAC812 is an ultra-fast-settling 12-bit current-output D/A converter with TTL-compatible inputs packaged in a 24-pin dual-wide dual-in-line hermetic metal package.

The current output settles to ±0.012% of full scale range in 55nsec, typical (65nsec, max., C grade; 80nsec, max., B grade).

The DAC812 utilizes a monolithic 12-bit switch chip with stable, compatible thin-film resistors to achieve fast settling time and excellent stability over temperature and time. An internal applications resistor for use with an external op amp is included to convert the output current into a voltage for 0V to +10V or −5V to +5V ranges.

An output voltage compliance range of +4V to −4V allows the generation of an output voltage without using an external output amplifier.

The DAC812 comes in two drift grades. The linearity error of the C grade is guaranteed to be within ±1/2LSB over the temperature range of −25°C to +85°C. Gain drift of the C grade is ±20ppm/°C (max) and bipolar offset drift is ±10ppm of FSR/°C (max). The B grade has a linearity error of ±1LSB over the temperature range and a maximum gain drift and bipolar offset drift of ±40ppm/°C and ±15ppm/°C, respectively.

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PDS-509C

SPECIFICATIONS

ELECTRICAL

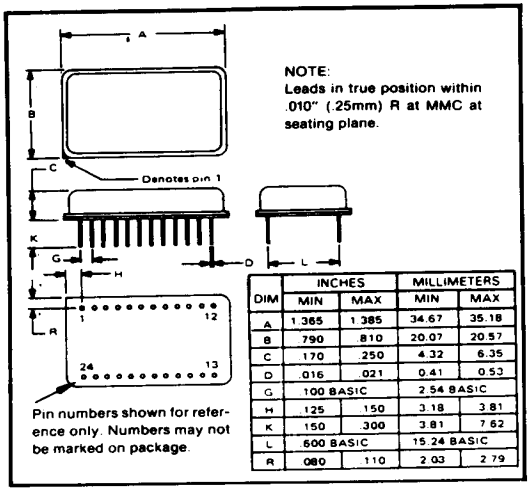
At T_A = +25°C, rated power supplies, and after 5-minute warm-up unless otherwise noted.

MODEL	DAC812CM			DAC812BM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT							
DIGITAL INPUT							
Resolution; CSB, COB			12			*	Bits
Logic Inputs: V_{IH}	+2.0		+5.25	*		*	V
V_{IL}	0.0		+0.8	*		*	V
I_{IH}, V_I = +2.7V			+40			*	µA
I_{IL}, V_I = +0.4V			−1.8			*	mA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error		±0.006	±0.012		±0.009	±0.018	% of FSR[1]
Differential Linearity Error			±0.012			±0.018	% of FSR
Gain Error[2]		±0.03	±0.1		*	*	%
Offset Error[2]: Unipolar		±0.02	±0.04		*	*	% of FSR
Bipolar		±0.03	±0.1		*	*	% of FSR
Monotonicity Temp. Range (min)	−25		+85	*		*	°C
CONVERSION SPEED							
Settling Time to ±1/2LSB into 150Ω							
For FSR Change		55	65		*	80	nsec
For 1LSB Change		25			*		nsec
DRIFT							
Gain		±10	±20		±20	±40	ppm/°C
Offset: Unipolar		±0.25	±0.5		±0.5	±1	ppm of FSR/°C
Bipolar			±10			±15	ppm of FSR/°C
Linearity Error	±0.012 over Temp. Range (max)			±0.025 over Temp. Range (max)			% of FSR
Differential Linearity Error	±0.025 over Temp Range (max)			±0.04 over Temp. Range (max)			% of FSR
OUTPUT							
ANALOG OUTPUT							
Output Current: Unipolar		0 to −10			*		mA
Bipolar		−5 to +5			*		mA
Output Voltage Ranges							
with External Op Amp: Unipolar		0 to +10			*		V
Bipolar		−5 to +5			*		V
Output Impedance: Unipolar		170			*		Ω
Bipolar		150			*		Ω
Output Compliance	−4		+4	*		*	V
POWER SUPPLIES							
Power Supply Sensitivity: $+V_{CC}$			±0.004			*	%FSR/%V_{CC}
$-V_{CC}$			±0.001			*	%FSR/%V_{CC}
V_{DD}			±0.0002			*	%FSR/%V_{DD}
Power Supply Voltages: $+V_{CC}$	+11.4	+15	+18	*	*	*	V
$-V_{CC}$	−18	−15	−14	*	*	*	V
V_{DD}	+4.5	+5	+5.5	*	*	*	V
Power Supply Current: $+V_{CC}$		+30	+40		*	*	mA
$-V_{CC}$		−40	−50		*	*	mA
V_{DD}		+25	+40		*	*	mA
Power Dissipation		1.2	1.6		*	*	W
PHYSICAL CHARACTERISTICS							
TEMPERATURE RANGE							
Specification	−25		+85	*		*	°C
Storage	−55		+150	*		*	°C
PACKAGE	24-pin Hermetic Metal DIP 0.6" Pin Row Spacing						

*Specification the same as for DAC812CM.

NOTES: (1) FSR is full-scale range. (2) Adjustable to zero with external potentiometer. Gain error is specified for unadjusted operation using internal resistor network. See Figure 5 and Figure 6.

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

PIN ASSIGNMENTS

Pin	Function	Pin	Function
1	Bit 1 (MSB, Data Input)	14	Digital Common (V_{DD} Common)
2	Bit 2	15	Analog Common ($\pm V_{CC}$ Common)
3	Bit 3	16	Analog Common
4	Bit 4	17	Analog Common
5	Bit 5	18	Analog Common
6	Bit 6	19	V_{DD} (Logic Supply)
7	Bit 7	20	I_{OUT} (Current Output)
8	Bit 8	21	R_f (Application Resistor)
9	Bit 9	22	BPO (Bipolar Offset)
10	Bit 10	23	$-V_{CC}$ (Negative Analog Supply)
11	Bit 11	24	$+V_{CC}$ (Positive Analog Supply)
12	Bit 12 (LSB)		
13	No connection		

DISCUSSION OF SPECIFICATIONS

ACCURACY

Linearity of a D/A converter is one of the true measures of its performance. The linearity error of the DAC812 is specified over its entire temperature range. The analog output will not vary by more than ±1/2LSB (±1LSB for the BM model) from a best-fit straight line over the specified temperature range of −25°C to +85°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a −25°C to +85°C range is guaranteed to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by 1) testing the end point differences for the DAC812 at t_{min}, +25°C, and t_{max}; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications (includes internal reference).

Offset Drift is a measure of the actual change in output around the minus full-scale point over the specified temperature range. The offset is measured at t_{min}, +25°C, and t_{max}. The maximum change in Offset is referenced to the Offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of the DAC812 is ±4.0V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages. To insure precision operation, each supply lead should be bypassed to ground as close to the unit as possible with a 1μF CS-type tantalum capacitor.

GROUNDING

Care must be exercised when grounding the DAC812 (pins 14, 15, 16, 17, and 18). In order to preserve the stated linearity and accuracy specifications it is necessary to use the ground pins as the analog ground reference point. Any voltage drop that develops between any of these five pins and the actual ground reference point will degrade the performance of the DAC812. To achieve fast settling performance it is recommended that pins 14 through 18 be returned directly to a ground plane (see Figure 1). The analog ground should be located as close to the DAC812 as possible. Otherwise, the accuracy will be degraded by the voltage drop in the ground lines.

SETTLING TIME

Settling time for the DAC812 is the total time required for the output to settle within an error band around its

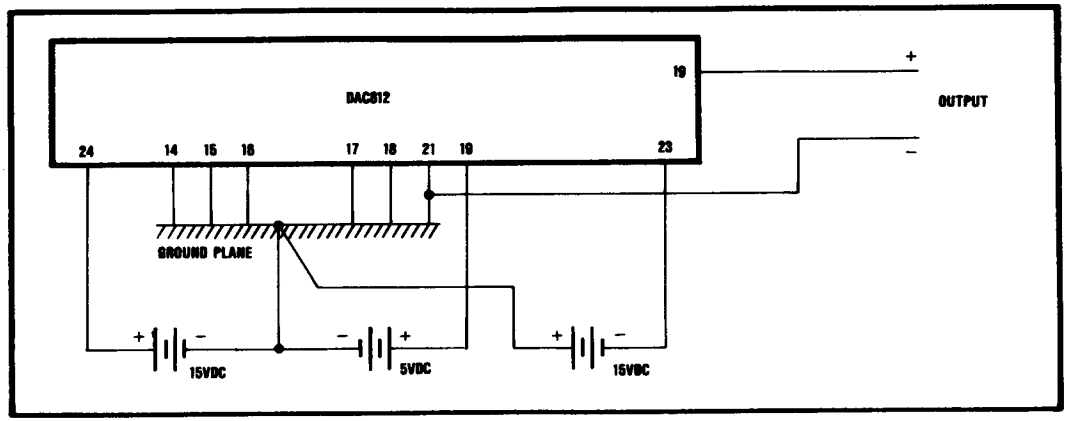


FIGURE 1. DAC812 Grounding Using Feedback Resistor to Generate Output Voltage.

final value after a digital input change. This time includes the digital delay of the internal switches.

Figure 2 shows a typical settling time curve of the DAC812 versus output error. This curve is for full-scale digital code changes. Figures 3 and 4 show typical measured settling time characteristics of the DAC812.

In order to achieve the minimum settling time, it is necessary to observe the following good high frequency construction techniques.

1. The power supplies should be bypassed by 1μF CS-type tantalum capacitors.
2. Use a ground plane to connect common ground points.
3. Remove the ground plane from underneath signal lines where it would add capacitance.
4. Keep analog and digital signal lines physically separated to avoid coupling of the digital signal into the analog paths.

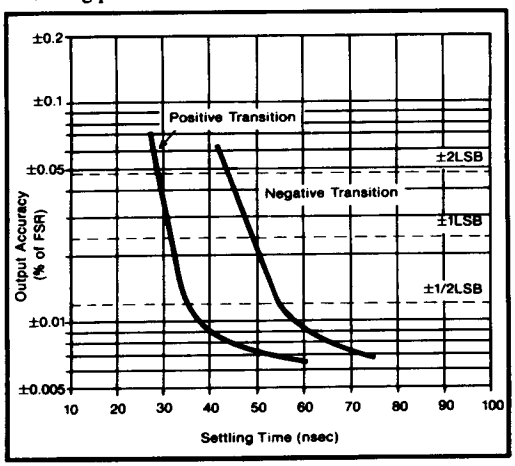


FIGURE 2. DAC812 Typical Settling Time vs. Accuracy

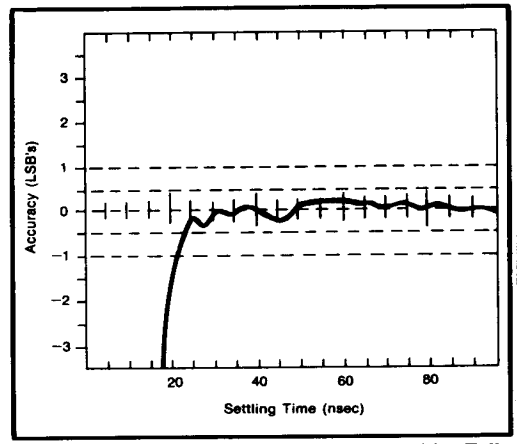


FIGURE 3. Typical DAC812 Negative-to-Positive Full-Scale Output Characteristic.

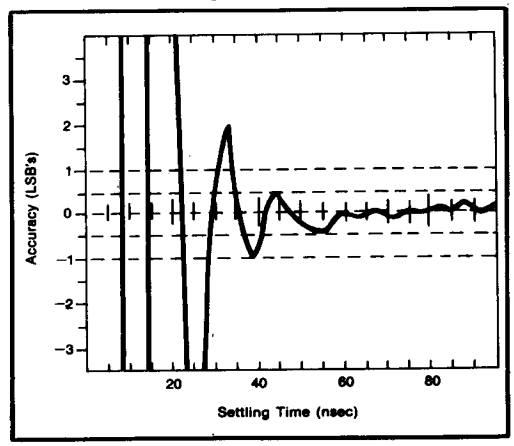


FIGURE 4. Typical Positive-to-Negative Full-Scale Output Characteristic.

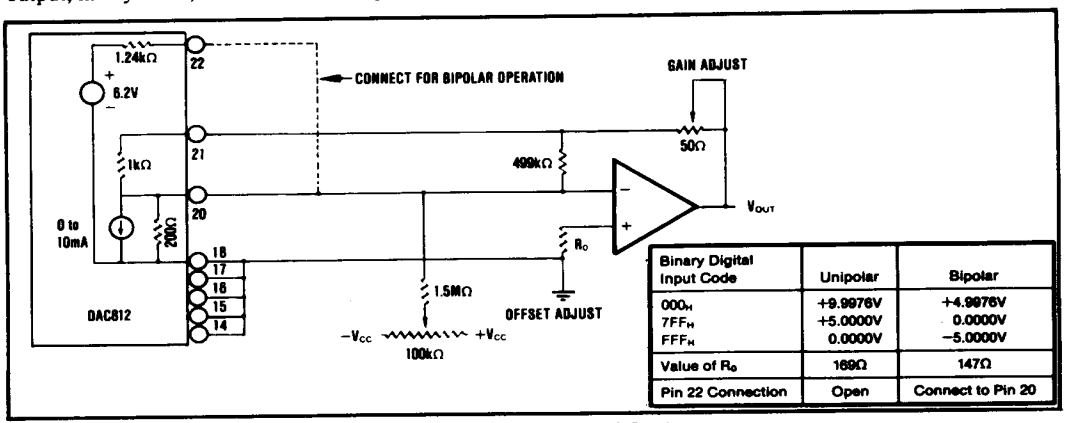
5. Bring the source of the digital driving signal as close to the inputs of the DAC812 as possible. If the digital inputs are not clean it will be necessary to reshape them using registers or line drivers. It is recommended that the logic power line be bypassed near the digital logic circuitry as a further measure to achieve clean signals.
6. If possible, the DAC812 should be soldered directly into the printed circuit board since connector lead length will cause ringing in the output.

OUTPUT CONFIGURATIONS AND APPLICATIONS INFORMATION

The DAC812 contains a 1.24kΩ resistor for generating the bipolar offset current and a 1kΩ resistor which is used as the feedback resistor when used with an external op amp. This thin-film network is constructed on sapphire to provide excellent temperature tracking capability inherent in thin-film networks. These internal resistors along with other internal resistors cause the DAC812 output, in any mode, to be a ratiometric product of the reference. The feedback resistor has very low power sensitivity so that linearity is maintained independent of digital-code changes. Because this resistor is constructed on a sapphire network, it is possible to have both superior tracking and low capacitance.

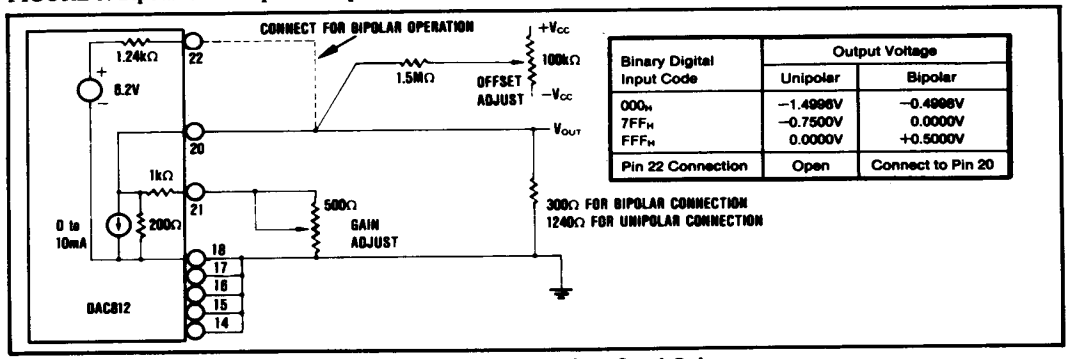
Figure 5 shows the DAC812 connected to an external op amp in unipolar and bipolar modes. When the op amp is a Burr-Brown model OPA600 it is possible to achieve settling times to 0.1% accuracy in 150nsec. Output accuracy and linearity specifications are given when connected to an external op amp.

For highest speed operation, the DAC812 should be used without an external op amp. Figure 6 shows how to connect the DAC812 for bipolar and unipolar operation. Figure 7 illustrates how to connect the DAC812 to construct a fast A/D converter.



Binary Digital Input Code	Unipolar	Bipolar
000_H	+9.9976V	+4.9976V
$7FF_H$	+5.0000V	0.0000V
FFF_H	0.0000V	−5.0000V
Value of R_o	169Ω	147Ω
Pin 22 Connection	Open	Connect to Pin 20

FIGURE 5. Bipolar and Unipolar Output Connections with External Op Amp.



Binary Digital Input Code	Output Voltage	
	Unipolar	Bipolar
000_H	−1.4996V	−0.4998V
$7FF_H$	−0.7500V	0.0000V
FFF_H	0.0000V	+0.5000V
Pin 22 Connection	Open	Connect to Pin 20

FIGURE 6. Bipolar and Unipolar Output Connection with Resistor Load Only.

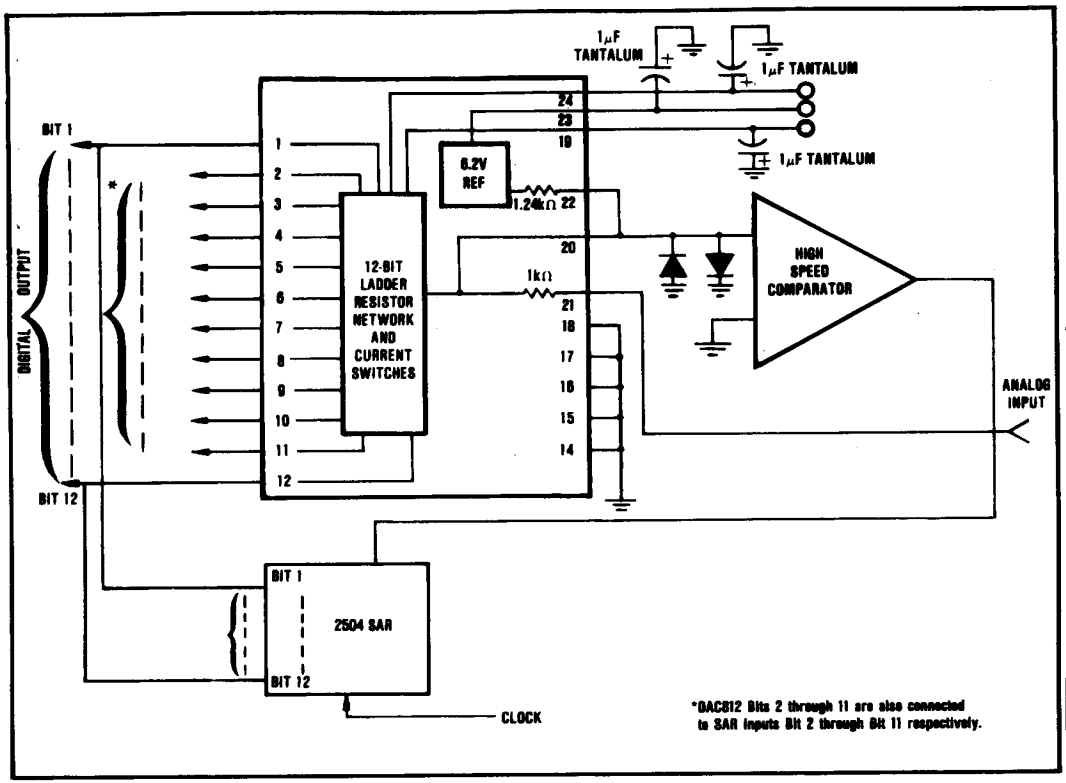


FIGURE 7. DAC812 Used in a Fast A/D Converter.