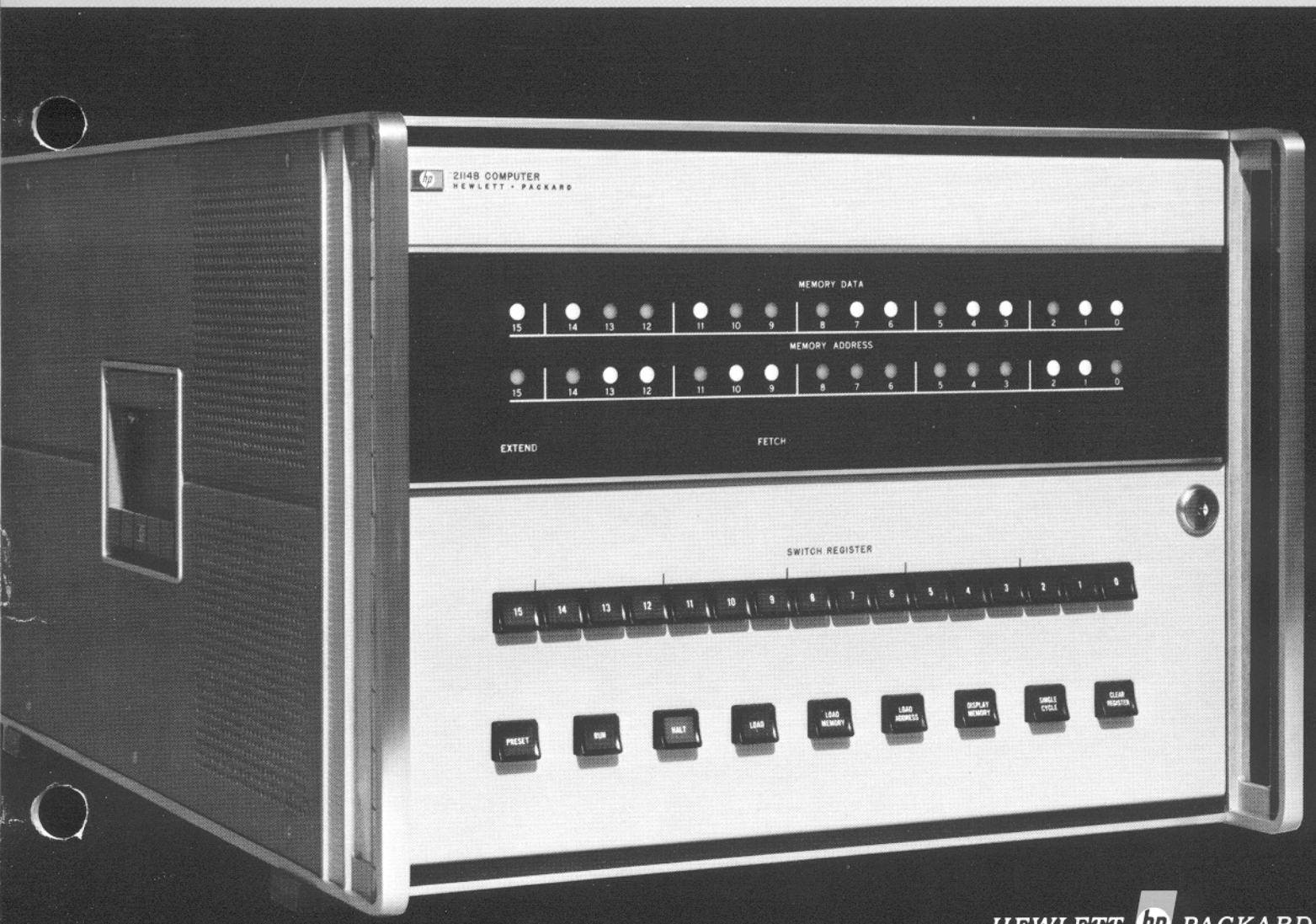
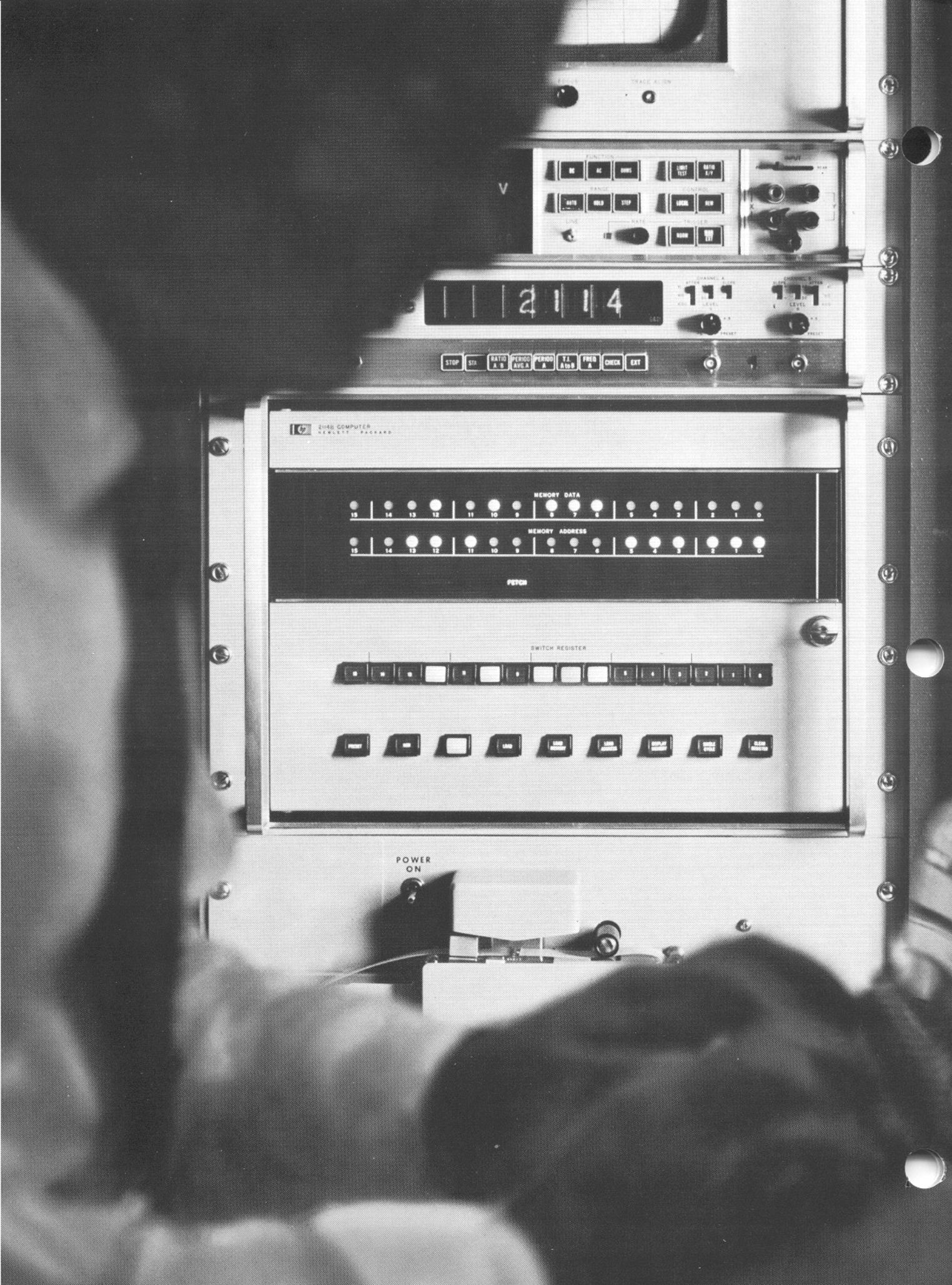
2114B COMPUTER



HEWLETT hp PACKARD

DIGITAL COMPUTERS


2114
STOP
STA
RATIO A/B
PERIOD AVG A
PERIOD A
T.I. A to B
FREQ A
CHECK
EXT
2114B COMPUTER
HEWLETT PACKARD
MEMORY DATA
MEMORY ADDRESS
FETCH
SWITCH REGISTER
POWER
ON

2114B OFFERS

Big computer performance and small computer versatility

GENERAL

Modular hardware and software
Compact table-top or rack mounted cabinet
CTL and TTL integrated circuits

PROCESSOR

70 powerful one-word instructions
Combining (microprogramming) of up to 8 instructions
Two addressable accumulators to simplify programming
Unlimited levels of indirect addressing allowed
Registers and memory contents readily modified or displayed from console

MEMORY

16-bit word size – 17th bit accessible with Plug-in parity option
4,096 or 8,192 (optional) word memory
2.0 microsecond full cycle time
Protected 64-word block for stored loader
Large 1024-word page size
Directly address two pages, indirectly address any page

INPUT/OUTPUT

7 plug-in I/O channels in mainframe plus 17 additional channels with I/O Extender unit
Optional high-speed Direct Memory Access channel
Peripherals interfaced simply with plug-in cards
Interface cards for many digital instruments and peripherals
Optional multiplexed I/O system allows interfacing up to 56 devices
High speed I/O channel (optional) for use with multiplexed I/O system

SOFTWARE

Two-pass ASA Basic FORTRAN (extended) or Assembly language programming
Basic Control System (BCS) for I/O flexibility
Modular I/O drivers for device independent programming
Linking Relocating Loader – links programs at load time
FORTRAN library accessible at compiler or assembly level
ALGOL and BASIC compilers for 8K systems
Modular Debug package – for on-line program debugging
Symbolic Editor, Prepare BCS, SIO Dump and hardware diagnostics

The HP 2114B is a stored program general purpose computer. It combines the most desirable computer features into a small, low-priced package. Up to 8K of memory, 7 device interface cards (plus optional DMA channel) and all power supplies are housed in a single, small cabinet. High-speed, software-flexibility, and expandable construction make the 2114B ideally suited for use as a general-purpose computer in a wide variety of systems applications. In addition, every 2114B is built to the high-quality standards you expect from Hewlett-Packard, assuring maximum performance and reliability.

SUPPLIED COMPLETE

Software and interface engineering for the 2114B is complete, built into the 2114B package, ready to go to work on your application. The HP 2114B has full compatibility with HP data measuring and recording instruments as well as a full range of standard computer peripherals. Peripherals include all interface electronics, cabling and software, eliminating any expensive installation or programming costs. General-purpose interface cards offer a wide latitude in configuring your system for special applications. Included in the low price of the 2114B are a 4K memory and all applicable software.

APPLICATIONS

The flexibility of the 2114B makes it ideal for use in either general-purpose computer systems or in specific systems applications such as process control, automatic checkout, data acquisition or data communication. Systems using standard HP computer peripherals and/or instruments are fully configured assuring complete hardware and software integrity. Hewlett-Packard also offers the industry's most straight-forward machine organization and input/output structure to permit ease of integration for special applications. Let your Hewlett-Packard computer specialist show you the advantages of using these features to solve your computer needs.

FULLY SOFTWARE SUPPORTED

HP provides complete, proven software for the 2114B. The standard software package includes FORTRAN, and Assembly language compilers, Basic Control System, Symbolic Editor, FORTRAN Library, System Input/Output and hardware diagnostics. All are operable with the minimum 2114B system configuration, i.e., 4K memory and Teleprinter input/output. For 8K systems Hewlett-Packard offers BASIC and ALGOL compilers. Field-proven capability plus complete documentation ensures a minimum of software overhead.

Specifications

MEMORY

Type: Magnetic core
Size: 4096 16-bit words (8192 words optional)
Page Size: 1024 words
Direct Addressing: Current page and Base page (2048 words)
Indirect Addressing: All pages
Cycle Time: 2.0 microseconds
Stored Loader: Activated by "LOAD" switch; automatically protected after program is stored.
Parity Option: 1 plug-in card, checks parity of transferred words, interrupts if a fault occurs. Address of offending word accessible to programmer.
Arithmetic: Parallel, two's complement binary

ARITHMETIC

Parallel, two's complement binary

COMPUTE SPEED

	Microseconds
Add	4.0
Subtract	6.0
Multiply	150*
Divide	375*
Floating Point Add	1150*
Floating Point Subtract	1150*
Floating Point Multiply	936*
Floating Point Divide	1873*

*Subroutine — time approximate

REGISTERS

Accumulators: Two (A and B), 16 bits each. Directly addressable
Memory Control: Three (T, P, M), 16 bits each
Supplementary: Two (Overflow and Extend), one bit each
Manual Data: One 16-bit proximity-type switch register

INSTRUCTIONS

Memory Reference (2 cycle):	14
Register Reference (1 cycle, micro-programmable):	43
Input/Output:	13
Total:	70

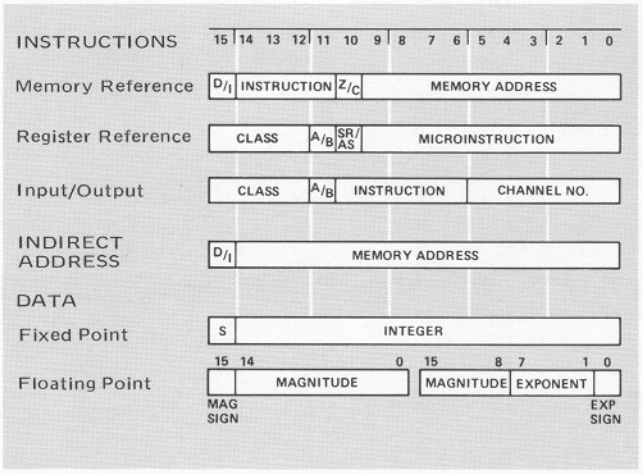
INPUT/OUTPUT

Number of prewired input/output slots in mainframe	7
Maximum number of I/O slots when used with 2151 I/O Extender	24
Total number of channels with optional I/O system	56

POWER FAIL INTERRUPT WITH AUTOMATIC RESTART (OPTION 08)

Interrupt Priority: Highest priority interrupt channel
Failure Subroutine: Automatically shifts control to a power failure subroutine which can save the contents of all computer registers in the event of power failure.
Automatic Restart: Restoring power causes execution of restart procedure returning control to the user's program.

WORD FORMATS



D/I DIRECT/INDIRECT; Z/C PAGE ZERO/CURRENT; A/B REGISTER IDENTIFIER; SR/AS SHIFT-ROTATE/ALTER-SKIP IDENTIFIER

DIRECT MEMORY ACCESS (ACCESSORY NO. 12607)

Capacity: Single channel (Computer slot A16)
Maximum Data Transfer Rate: 500,000 16-bit words/second
8-Bit Byte Transfer Time: 2 microseconds (Does not pack bytes)
16-Bit Word Transfer Time: 2 microseconds
Block Transfer Length: 1 to 8192 16-bit words
Cycles Required to Initiate Block Transfer: 6
Cycles Stolen from Main Program per word transferred: 1

HIGH SPEED I/O CHANNEL (ACCESSORY NO. 12616)

Capacity: Single input/output channel (computer slot A16) for use with multiplexed I/O (Accessory No. 12595 — External addressing of 56 different devices through the 2114B I/O control card).
Maximum Data Transfer Rate: 500,000 16-bit words/second
8-Bit Byte Transfer Time: 2 microseconds
16-Bit Word Transfer Time: 2 microseconds, maximum of 2.5 microseconds from request to complete transfer.
Block Transfer Length: 1 to 8192 16-bit words
Cycles Required to Initiate Block Transfer: 1
Cycles Stolen from Main Program per word transferred: 1
Memory Addressing: Random access to any location in core or sequential access from a specific starting address. Address register loaded externally.

MULTIPLEXED I/O OPTION (ACCESSORY NO. 12595)

Number of possible external devices: 56
Data Transfer: Bidirectional through the computer's input/output (IOB) lines.
Driver and Receiver Gates: OR-tieable through the user's controller
Signal Timing and Delays: Must be synchronized with the 2114 I/O backplane.
High Speed I/O: Can be used with high speed I/O channel (Accessory No. 12616)
Priorities: Uses either the mainframe I/O priorities or the addresses added by multiplexed I/O

MEMORY PARITY CHECK WITH INTERRUPT (ACCESSORY NO. 12598)

Checks: Verifies parity of all words transferred in or out of memory.

Indication: Front panel parity error indicator

Response: Selected computer response provides for either the parity error halt mode or the parity error interrupt mode.

Interrupt Response: Stores memory location of parity error for either mode of parity operation.

Parity Error Subroutine: Subroutine accessed through interrupt location corrects lost or added bit and returns control to main program.

PHYSICAL SPECIFICATIONS

Ventilation. Intake at rear, exhaust at sides. 2 inch recommended minimum exhaust clearance at sides.

Installation. May be used on table, or installed in standard 19-inch rack with furnished rackmount adapters.

Dimensions. 12 inches (304,8mm) high, 16-3/4 inches (425,5mm) wide, 24-3/8 inches (619,1mm) deep

Weight. Net 102 lb (48 kg), shipping 150 lb (68 kg)

Power Required. 115V (7 amp.) ± 10%, 50 to 60 Hz. 230V (3.5 amp.) operation requires external transformer.

Power Consumption. 500W minimum (with Teleprinter Option) to 800W maximum depending on number of I/O interfaces installed.

Environmental Conditions

Ambient Temperature

Standard: +10 to +40°C (+50 to +104°F)

Wide Temperature Option: 0 to 50°C (+32 to 122°F)

Relative Humidity

Standard: 80% at 40°C

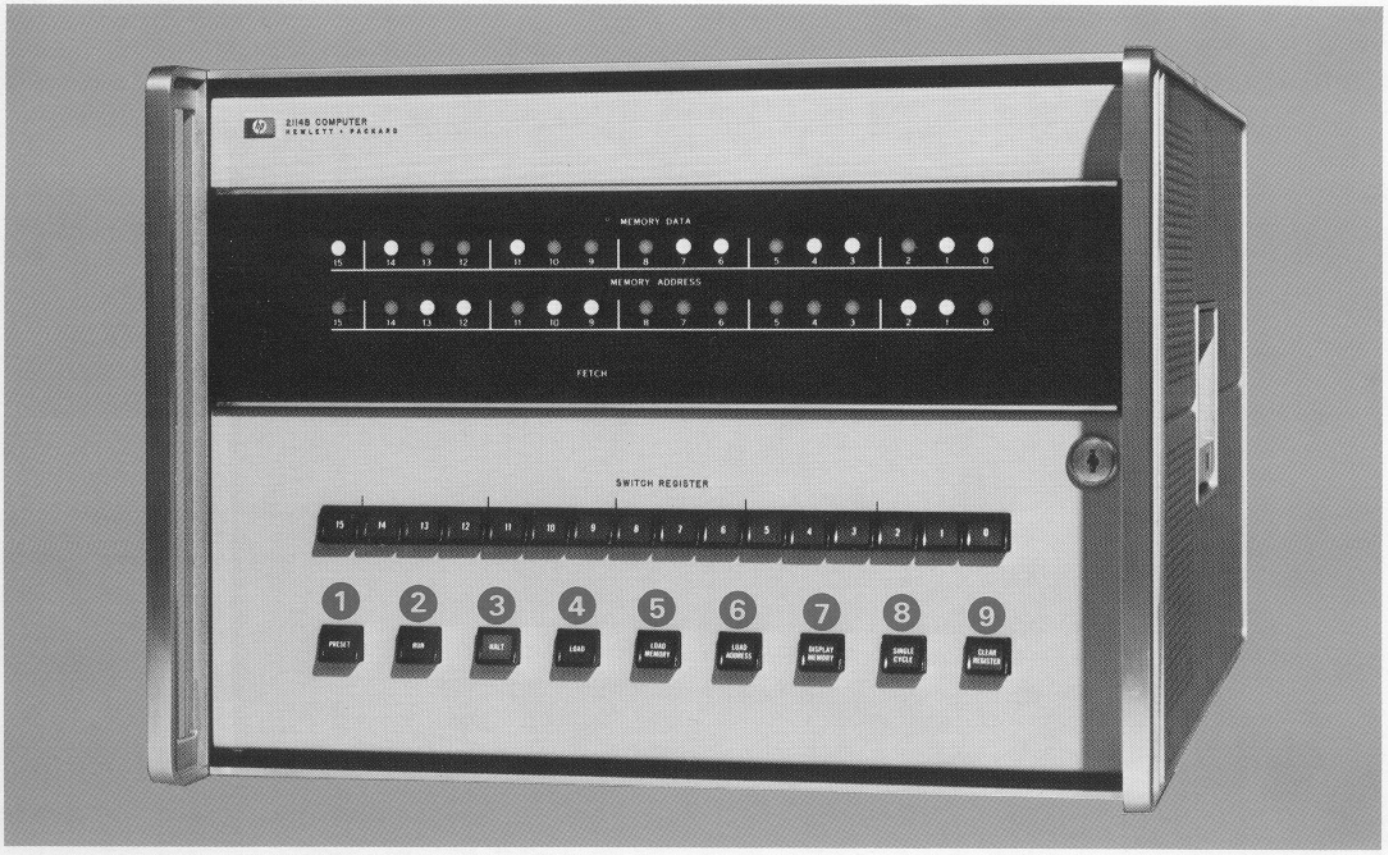
Wide Temperature Option: 80% at 50°C

CONSOLE CONTROLS (Illuminated when 'on')

1. **PRESET.** Presets the computer to Fetch phase, turns off interrupt system, resets parity error indication.
2. **RUN.** Starts operation at the current state of the registers.
3. **HALT.** Stops computer operation at end of current phase.
4. **LOAD.** Sets program counter to starting address of Absolute Binary Loader; enables and activates the protected Loader which then loads a program into memory; detects a computer halt after the program is loaded and protects the loader. The ultimate in ease of loading for a small computer.
5. **LOAD MEMORY.** Transfers Switch Register contents into the memory location specified by the M-Register.
6. **LOAD ADDRESS.** Transfers Switch Register contents into the Memory Address Register and Program Counter.
7. **DISPLAY MEMORY.** Displays in the Memory Data Register the contents of the address specified in the Memory Address Register.
8. **SINGLE CYCLE.** Steps program one machine cycle.
9. **CLEAR REGISTER.** Clears switch register to all zeros.

PROTECTED CONTROLS

POWER SWITCH, MANUAL LOADER ENABLE/DISABLE, LAMP TEST, CONSOLE SWITCHES ENABLE/DISABLE, and DIAGNOSTIC SWITCHES are all located behind the lockable, hinged panel. Protects your programs when you're not around.



Processor organization

CONSOLE REGISTERS

MEMORY ADDRESS (M). Holds the address of the memory word to be accessed.

MEMORY DATA (T). Displays information transferred in or out of memory.

EXTEND (E). One-bit register; used to link A or B registers, or to indicate a carry from A or B.

OVERFLOW (OV). One-bit register used to indicate a carry from A or B.

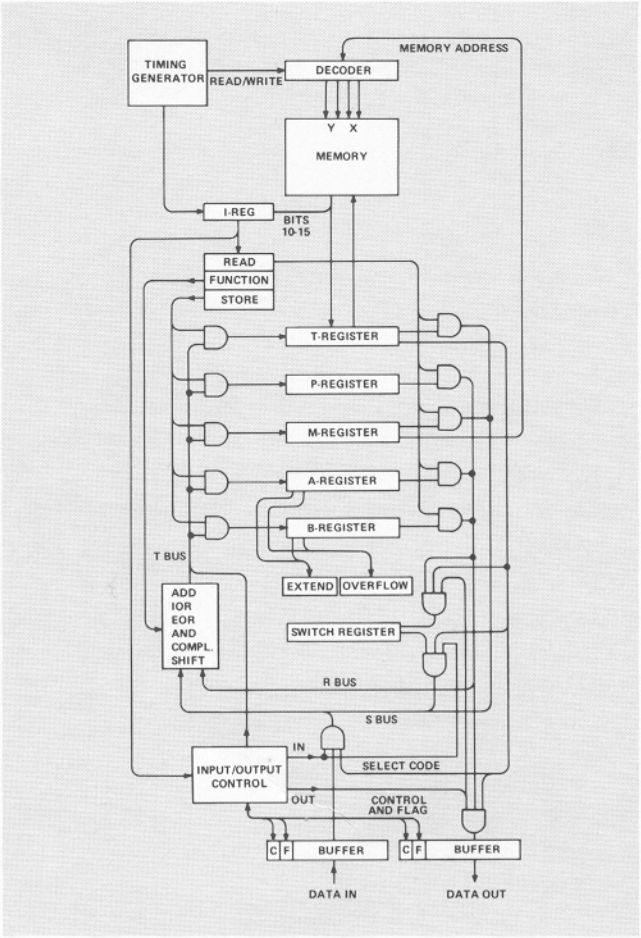
SWITCH REGISTER (S). Row of 16 proximity-sense switches manually transferable to A, B, P, M, or memory. By program, transferable to A or B, or A or B transferable to switch register, displayed through the lighted switches.

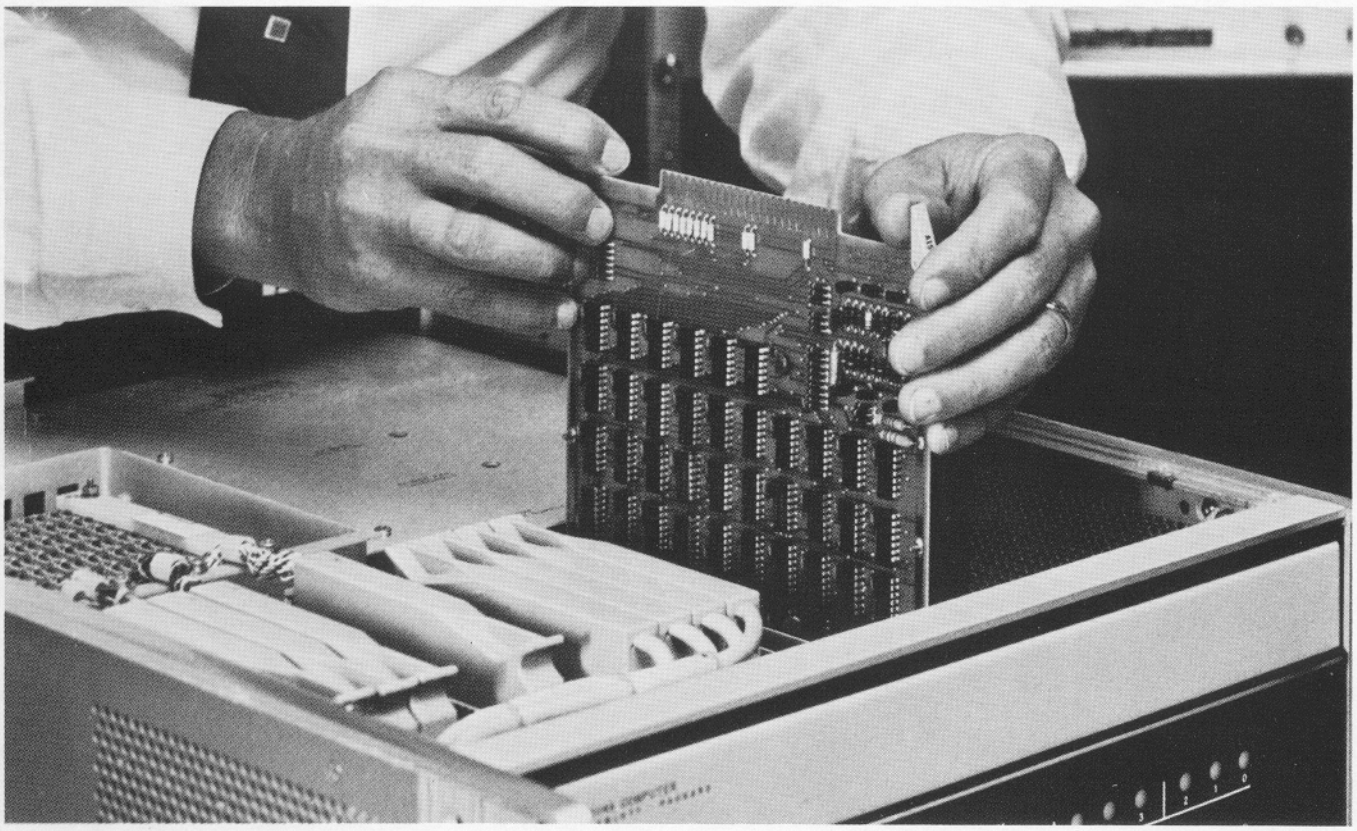
REGISTERS ACCESSIBLE FROM CONSOLE

A-REGISTER. Accumulates the results of arithmetic operations, and serves as a transfer register for input and output. Addressable as memory location 0 for additional flexibility. Displayed by examining location 0.

B-REGISTER. Second accumulator, same functions as the A-Register. Addressable as location 1. Displayed by examining location 1.

P-REGISTER. "Program Counter"; holds the address of the next instruction to be fetched from memory.





Instruction repertoire

The HP 2114B has 70 basic one-word (16-bit) instructions, executable in 2 or 4 microseconds (plus 2 microseconds for each level of indirect addressing). These instructions are grouped in three types: Memory Reference 14, Register Reference 43, Input/Output 13. Groups of up to 8 register reference instructions can be microprogrammed to form many useful additional one-word instructions, as shown in the table below.

TYPE	MNEMONIC	DESCRIPTION	μSEC
MEMORY REFERENCE (14)	AND	"And" (M) to A; result in A	4.0
	XOR	"Exclusive or" (M) to A; result in A	4.0
	IOR	"Inclusive or" (M) to A; result in A	4.0
	JSB	Jump to subroutine, save P	4.0
	JMP	Jump, unconditionally	2.0
	ISZ	Increment (M); skip if result zero	4.5
	ADA/B	Add (M) to A or B; result in A or B	4.0
	CPA/B	Compare (M) with A or B; skip if unequal	4.0
	LDA/B	Load (M) into A or B	4.0
	STA/B	Store A or B into M; A/B unchanged	4.0
REGISTER REFERENCE (43)		SHIFT-ROTATE GROUP	2.0
	NOP	No operation	
	CLE	Clear E (Extend)	
	SLA/B	Skip if least significant bit of A/B is zero	
	A/BLS	A/B arithmetic left shift one bit	
	A/BRS	A/B arithmetic right shift one bit	
	RA/BL	Rotate A/B left one bit	
	RA/BR	Rotate A/B right one bit	
	A/BLR	A/B left shift one bit, sign cleared	
	ERA/B	Rotate E right one bit with A or B	
	ELA/B	Rotate E left one bit with A or B	
	A/BLF	Rotate A or B left four bits	
		ALTER-SKIP GROUP	2.0
	CLA/B	Clear A or B	
	CMA/B	Complement A/B (ones complement)	
	CCA/B	Clear-complement A/B (see to -1)	
	CLE	Clear E (Extend)	
	CME	Complement E	
	CCE	Clear-complement E (set E)	
	SEZ	Skip if E is zero	
	SSA/B	Skip if sign of A/B is zero (positive)	
	SLA/B	Skip if least significant bit of A/B is zero	
	INA/B	Increment A/B by one	
	SZA/B	Skip if A/B is zero	
	RSS	Reverse skip sense	
		OVERFLOW	2.0
	STO	Set overflow bit	
	CLO	Clear overflow bit	
	SOC	Skip if overflow bit clear	
	SOS	Skip if overflow bit set	
INPUT/OUTPUT (13)	HLT	Halt program	2.0
	STF	Set flag bit of selected I/O channel	
	CLF	Clear flag of selected I/O channel	
	SFC	Skip if flag clear	
	SFS	Skip if flag set	
	MIA/B	Merge ("or") I/O channel into A/B	
	LIA/B	Load I/O channel into A/B	
	OTA/B	Output A/B to I/O channel	
	STC	Set control bit of selected channel	
	CLC	Clear control bit of selected channel	

(M) = Contents of Memory Location M
Overflow Instructions coded under I/O group

MEMORY REFERENCE: Memory addressing of the HP 2114A is based on a 1024-word page structure. All memory reference instructions address either the current page or the base page, thus up to 2048 words are directly addressable. The large page size of the 2114B allows compact programs with a minimum of indirect addressing. Also, programs can share a large block of storage in the base page, easing communication between routines using common data bases. Accumulators are directly addressable as memory locations 0 and 1, enabling their contents to be added and compared. You can also load from one accumulator into the other.

REGISTER REFERENCE: The 2114B's extensive set of register reference instructions make it easy to edit character strings, shift data within and between accumulators, test the accumulators for condition (zero/non-zero, positive/negative, odd/even) and to clear, set, increment and form the one's and two's complement of the accumulator contents.

INPUT/OUTPUT: These instructions are used to control peripheral devices, transfer data to and from peripherals, and control the interrupt system. Data can be input and output directly from the A and B accumulators. You can also output to the illuminated switch register, a useful extension of the console register displays.

MICROINSTRUCTION COMBINING GUIDE FOR REGISTER REFERENCE INSTRUCTIONS

Combine one instruction in a column with any instructions in adjacent columns. (References to A and B registers cannot be mixed.) Example: ALS, CLE, ARS is executed in one machine cycle.

SHIFT-ROTATE GROUP

ALS ARS RAL RAR ALR ERA ELA ALF	CLE	SLA	ALS ARS RAL RAR ALR ERA ELA ALF
BLS BRS RBL RBR BLR ERB ELB BLF	CLE	SLB	BLS BRS RBL RBR BLR ERB ELB BLF

ALTER-SKIP GROUP

CLA CMA CCA	SEZ	CLE CME CCE	SSA	SLA	INA	SZA	RSS
CLB CMB CCB	SEZ	CLE SME CCE	SSB	SLB	INB	SZB	RSS

Typical uses for Microinstructions

Bit Testing RAR, SLA, RAL	Skip next instruction if bit 1 in the A register is zero.
Register Testing SEZ, SZA, RSS	Skip next instruction if either the E register or the A register is non-zero.

Input/output system

CAPACITY. Provides for seven 16-bit parallel channels contained on plug-in cards located in the computer mainframe. Seventeen additional I/O channels (for a total of 24 I/O channels) can be easily added by use of the optional 2151A I/O Extender. All Extender I/O channels may be addressed as if they were located in the mainframe. The Direct Memory Access channel is program assignable to any mainframe channel but not extender channels.

DATA TRANSFER. Multilevel priority interrupt capability is a standard hardware feature of the 2114B. Since many I/O devices may request servicing simultaneously each interface card slot is assigned a specific priority. The interrupt system acknowledges each request, and interrupts the program in progress to service the devices in order of priority. Additionally, all or only specific devices may be deleted from the interrupt system and operated under program control.

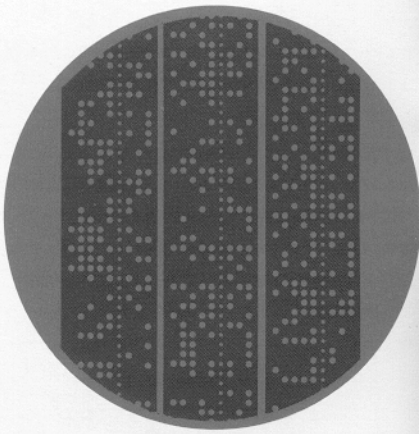
FLEXIBILITY. Most peripheral devices interface with a single card containing data buffering, flag, interrupt and priority circuit. You can add, delete, or interchange devices from one channel to another – simply by plugging the interface card into the desired slot. Identical pin assignments of the slots permit this flexibility. The modular software can be readily reconfigured to correspond to the hardware configuration. In addition to interfacing for specific devices, multi-purpose interfaces are also available.

DIRECT MEMORY ACCESS. The direct memory access (DMA) option transfers data directly to and from the computer memory rather than through the computer's arithmetic and control logic. The mode of transfer is called "cycle stealing" since only one machine cycle is required for the entire transfer. Under DMA control, data may be transferred between the computer memory and external devices at a rate of 500,000 16-bit words per second. This means that the range of computer capabilities may be extended to include applications where data is generated at rapid rates or in large quantities.

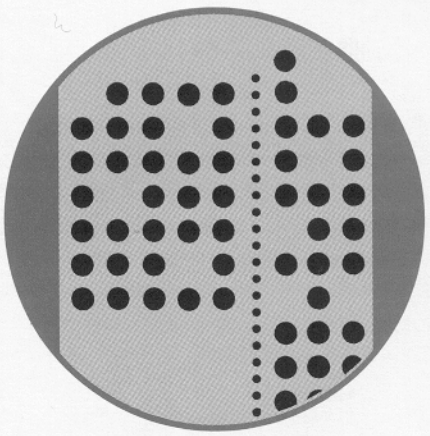
HIGH SPEED INPUT/OUTPUT. For multiplexing at high data rates the high speed I/O channel is available for use in conjunction with multiplexed I/O. The high speed option operates in a manner similar to DMA. Input/Output data is transferred via the multiplex card directly to or from memory using the "data break" transfer mode. At the maximum transfer rate of 500 KHz, the option is capable of stealing consecutive machine cycles until a block transfer is complete. By use of this sytem, fast devices can be controlled through the high speed channel while slower devices operate under program control.

MULTIPLEXED I/O SYSTEM. An optional interface card delivers all I/O addresses, I/O control and timing signals and data lines to the user. You can then construct your own interfaces to special devices, but still use the remaining I/O channels for standard plug-in interfaces to devices such as the teleprinter, tape reader, or magnetic tape unit. Depending in which slot you install the I/O multiplexer card, you have the capability of interfacing up to 56 addressable devices. All of these devices may be operated using the standard input/output instructions or under interrupt control from the multiplexed channel.

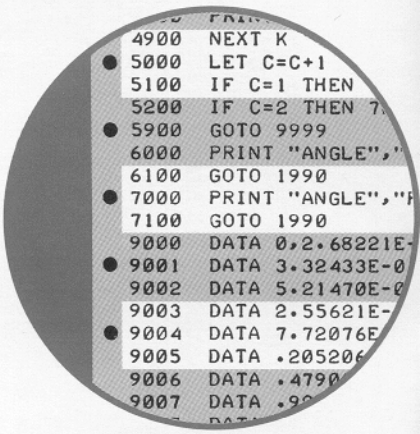
THE KIT CONCEPT. Input/output options are conveniently packaged as complete interface kits – including cards, cables software drivers and diagnostic programs. Additionally, where practical, the peripheral is included as part of the kit. Interface kits furnished with the original purchase are fully installed, tested, and delivered as a complete system. A complete list of input/output options (with prices) is available from your Hewlett-Packard field office.



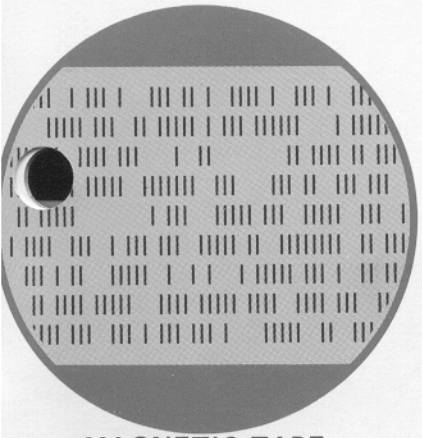
PUNCHED TAPE READER



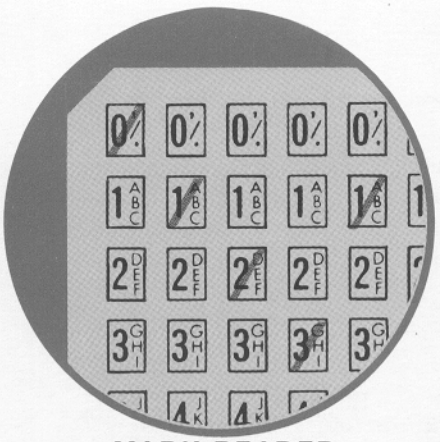
TAPE PUNCH



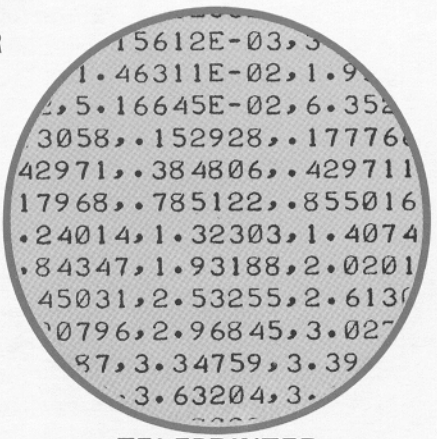
LINE PRINTER



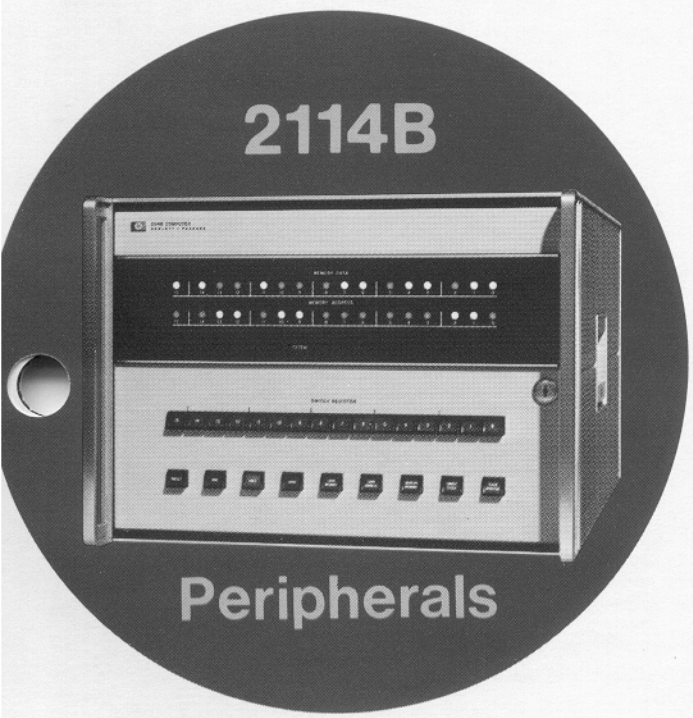
MAGNETIC TAPE

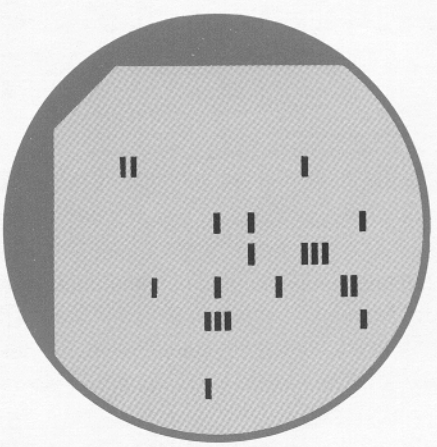


MARK READER

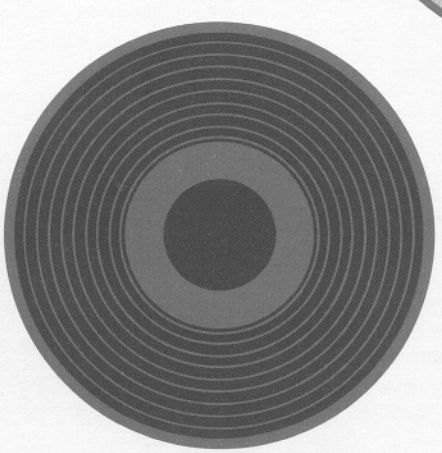


TELEPRINTER

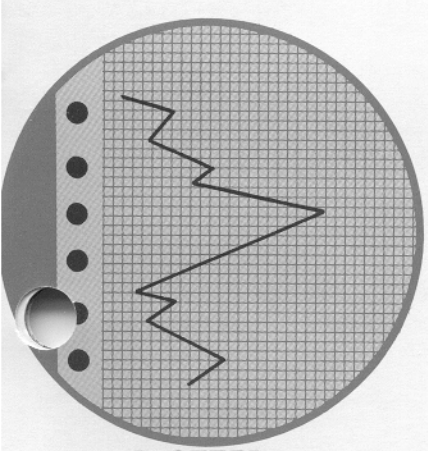




HIGH SPEED
CARD READER



DISC MEMORY OR DRUM



PLOTTER

Versatile and comprehensive software upward-compatible to bigger HP computers

FORTRAN

American Standards Association Basic FORTRAN
Allows problem description in a standardized mathematical language and provides efficient relocatable output plus

- Free Field Input — format need not be specified
- Hollerith Input/Output format of "..." eliminates character count
- Octal and alphanumeric format specifications
- Octal constants
- Two-branch IF
- Array declaration with a COMMON statement
- Redefinition of arguments by a function subprogram
- Basic External Functions for masking and Switch Register tests

ALGOL

Allows problem description in an internationally defined algorithmic language and produces a relocatable program in one pass. Requires 8K memory. Includes all major elements described in ALGOL 60 revised Report, Communications of the ACM, January 1963 — plus

- Intermixing of REAL and INTEGER identifiers in assignment statements
- Unrestricted nesting of conditional statements
- All variables treated as OWN variables
- Initialization of variables or arrays within type declaration
- Values assigned to variables with EQUATE declarations
- Logical unit designation in I/O statements
- HP FORTRAN format specifications for I/O, or Free Field Input data

BASIC

Accepts a simple mathematical language which has certain similarities to both FORTRAN and ALGOL. The BASIC system is an interpretative compiler; the program is compiled in memory and then executed immediately. Requires 8K and includes

- COM statement, to pass information blocks from one program to another
- CALL statement, to use assembly language subroutines and special purpose I/O device drivers
- WAIT statement, to temporarily delay program execution

ASSEMBLY LANGUAGE

Assembly language processes a machine oriented language providing the full flexibility of the hardware instructions. The language includes machine operation codes, assembler-directing pseudo codes, and symbolic addressing. The output may be absolute or relocatable. Linkable to FORTRAN code plus it includes

- Page-free programming — BCS provides indirect addresses
- Inter-program communication by EXTernal references and ENTry points
- Storage area reservation by BSS or COM statement
- Fixed and floating point arithmetic pseudo operations
- Absolute or relocatable output feature

EXTENDED ASSEMBLY

Provides additional capabilities for the 8K user — including

- Literal values as operands
- Output listing control pseudo operations

BASIC CONTROL SYSTEM (BCS)

Handles loading, relocating, and linking of user programs and library subroutines. Simplifies programming and execution of all input/output operations.

- Relocating Loader, to load, link, and initiate execution of relocatable object programs and library subroutines
- Absolute output Loader, to produce complete absolute binary output tapes for "production" programs
- Input/Output Control, to provide I/O operations with: software buffering, simple calling sequence, logical I/O unit numbers
- Input/Output Drivers, to perform actual I/O operations on all peripheral devices
- Prepare Control System, to generate BCS tape for a particular hardware configuration

DEBUGGING ROUTINE

Provides data on program operating during the check-out phase of program development. It simplifies and speeds up the process of getting the user's program running correctly.

- Dump specified areas of memory in octal or ASCII format
- Trace selected areas of program during execution
- Modify registers and selected areas of memory
- Specify operand and instruction breakpoint halts
- Initiate or continue program execution at any point

SYMBOLIC EDITOR

Simplifies the correction of a source program on paper tape. Inserts, deletes, or replaces characters or records from a symbolic file or source program tape.

PROGRAM LIBRARY

Makes available a quantity of frequently used computational procedures.

- Fixed-point multiply and divide
- Floating-point add, subtract, multiply, divide
- Double-word load and store
- Integer/real and real/integer conversions
- Exponential, natural log, sine, cosine, tan, tanh, arctan, square root
- Boolean functions — AND, OR, NOT
- Test individual switches of Switch Register
- Formatted I/O operations
- Position magnetic tape — skip records or files
- Generate lines and curves on a plotter

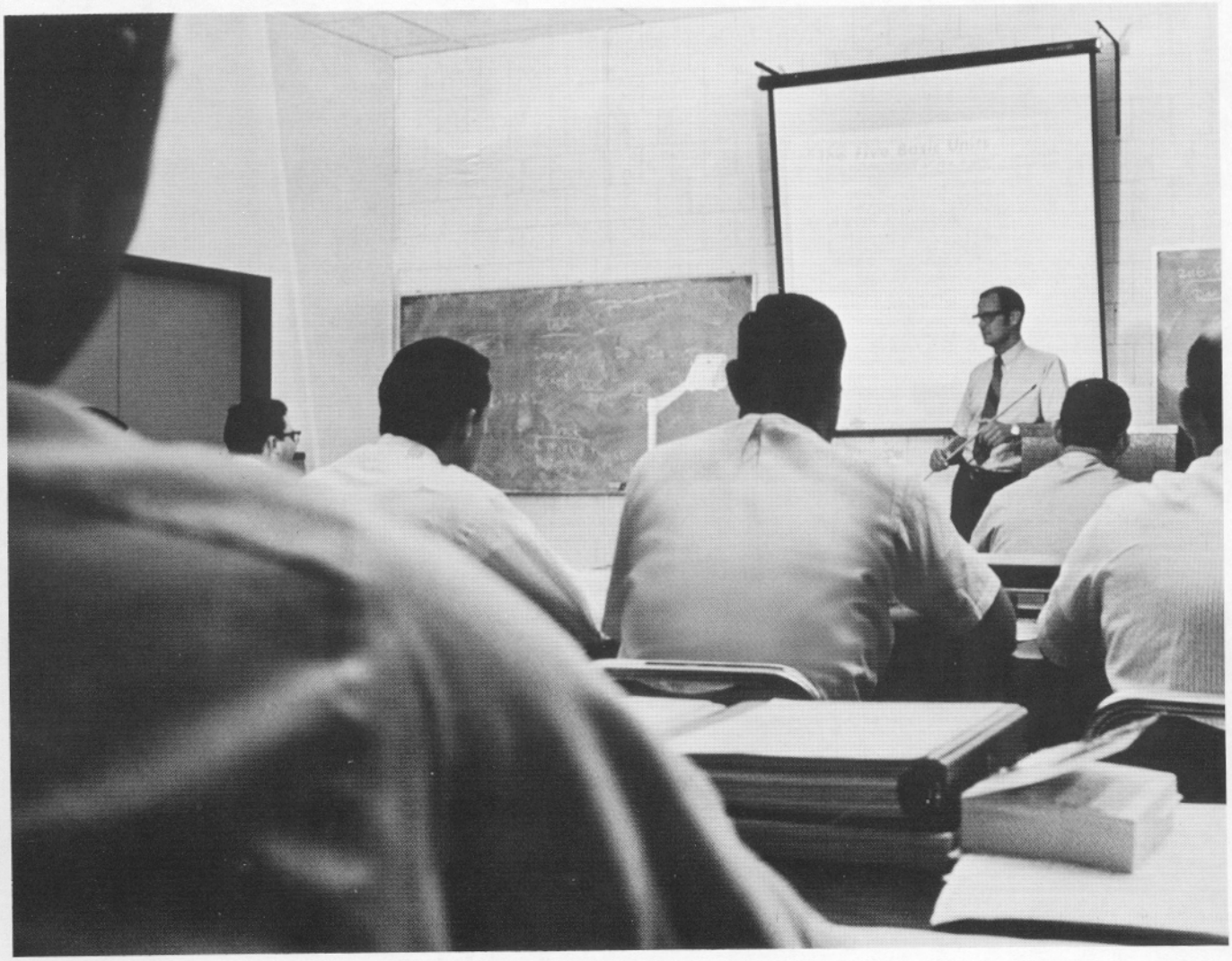
MAGNETIC TAPE SYSTEM

Utilizes a magnetic tape unit to provide vastly increased assembly, compilation and loading speed. Requires 8K memory.

FORTRAN, ALGOL, Assembly Language, Symbolic Editor, and

- Basic Control System software
- Batch Processing Mode
- Modular for tailored configuration

Hewlett-Packard training and support



USER (PROGRAMMING) TRAINING

Hewlett-Packard provides a free user-programmer course for customers at the factory in Cupertino, California. Training materials are also provided at no charge. The complete User Training Course assumes no knowledge of computer programming or electronic systems operation. It covers instruction on programming languages and operating system. At least two full days are devoted to hands-on experience.

MAINTENANCE TRAINING

Regularly scheduled Maintenance Training courses for customers are also available at the factory in Cupertino, California. The course assumes familiarity with digital logic circuits and covers the following subjects in depth: computer organization, computer instructions, logic operation and timing, I/O interfaces, and fault diagnosis. A full-time staff of professional instructors insures complete coverage of each subject using proven methods of presentation.

DOCUMENTATION

Hewlett-Packard is known for the quality and thoroughness of its operating and service manuals. Documentation furnished with HP computer systems includes programmer's reference manuals for all software furnished, operating procedures and detailed technical descriptions with diagnostic and maintenance procedures for all hardware modules plus diagnostics for the overall system.

REPAIR AND PARTS SERVICE

Service and parts assistance are available from Hewlett-Packard field offices throughout the United States, Canada and Europe. Local office facilities are backed up by Regional Service Centers. Major parts warehouses are located in Mountain View, California and Rockaway, New Jersey. Board exchange programs for computers and other complex instruments enable systems to be returned to normal operation with minimal down-time.

CUSTOMER SERVICE AGREEMENTS

Customer service agreements are available to provide on-site preventive maintenance and repair. Assistance can range from 5-day service during normal working hours to 7 day, all-hours backup.