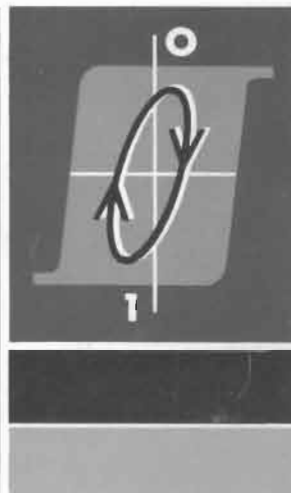
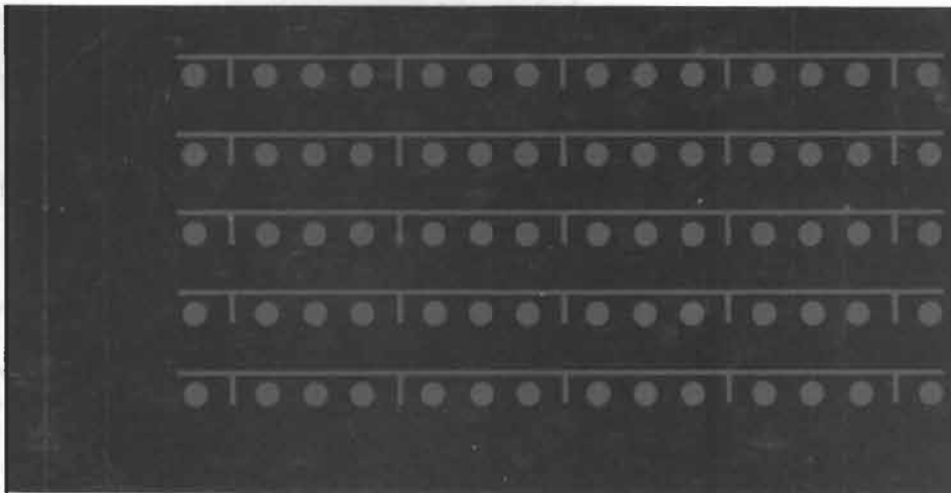




2114B COMPUTER

H E W L E T T • P A C K A R D



INPUT/OUTPUT SYSTEM OPERATION

VOLUME

3



**VOLUME THREE
INPUT/OUTPUT SYSTEM OPERATION MANUAL**

**MODEL 2114B
COMPUTER**



SERIAL NUMBERS PREFIXED: 930-, 942-, 943-, 947-, 949-

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Updating Supplement 1 May 1970

MANUAL IDENTIFICATION

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SUPPLEMENT DESCRIPTION

The purpose of this supplement is to correct manual errors (Errata) and to adapt the manual to instruments containing production improvements made subsequent to the printing of the manual. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left.

INSTRUMENT CHANGES

Prefix-Serial	Changes
942-	1
943-	1
947-	1
949-	1
972-	2

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Rev	Changes

CHANGE

DESCRIPTION

1. Change the title page of this manual to read "Serial Numbers Prefixed: 930-, 942-, 943-, 947-, 949-". No further changes to the manual are required to make it applicable to these serial number prefixes.
2. Add serial prefix 972- to the title page of this manual. No further changes to the manual are required to make it applicable to this serial prefix.

US-1

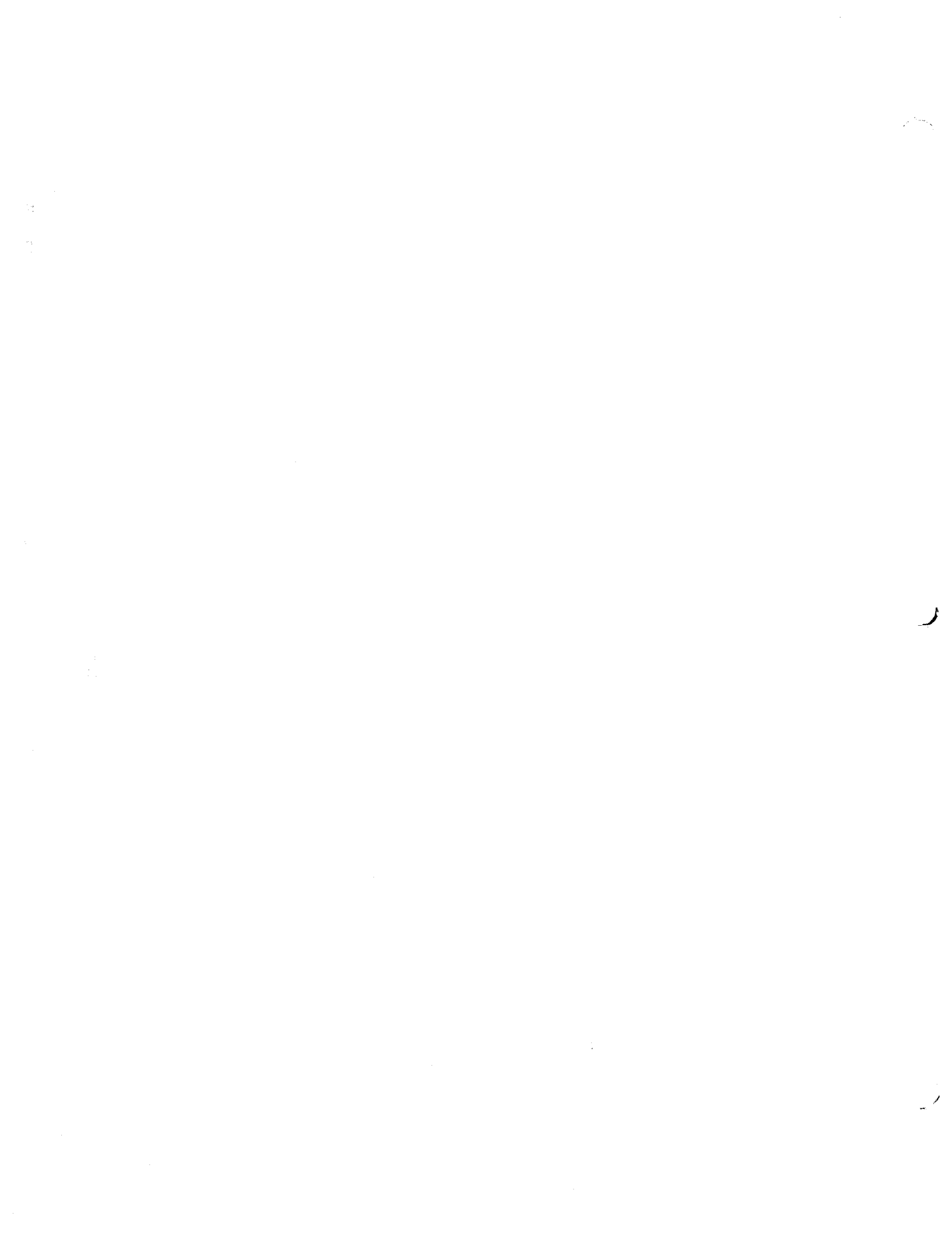


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Figure 1-1. Typical HP 2114B Computer System

SECTION I

INTRODUCTION

1-1. COMPUTER SYSTEM.

1-2. The computer system (figure 1-1) consists of the HP 2114B Computer, associated input/output devices, and the necessary interface logic and software.

1-3. The basic computer contains the facilities for control of up to seven peripheral devices. Plug-in processor options are available for expansion of computer capabilities, and a wide range of input/output options are available. Refer to volumes one and two of the HP 2114B Computer Manual for detailed information on the computer, and to volume four for programming information.

1-4. MANUAL CONTENTS.

1-5. This manual contains a description of the input/output structure in section II. Theory of operation and

logic diagrams for the I/O control card, including the I/O address circuits are contained in section III.

1-6. SUPPLEMENTAL MANUALS.

1-7. Operating and service manuals are provided with each I/O device and interface kit purchased. These manuals generally include the following information:

- a. General information.
- b. Installation and programming.
- c. Theory of operation.
- d. Troubleshooting and maintenance
- e. Replaceable parts lists and ordering information.

SECTION II

INPUT/OUTPUT STRUCTURE

2-1. INTRODUCTION.

2-2. The I/O structure of the HP 2114B Computer system consists of the I/O devices, their respective interface cards and interconnecting cables, and an I/O control card which contains the I/O control and address logic (see figure 2-1). The I/O section of the computer card rack consists of nine printed circuit card slots: seven for I/O interface cards and one each for the I/O control card and the optional direct memory access (DMA) card. Some I/O devices require only one interface card, while other I/O devices require two interface cards to interface the external device to the computer.

2-3. Functionally, the I/O structure allows the computer to select and communicate with each of the interface cards through the I/O control and address logic and through direct bus wiring. The I/O structure also provides a means by which I/O devices can interrupt the computer program in order to be serviced by the computer. When more than one device requests an interrupt, the computer processes the requests on a priority basis.

2-4. The number of I/O interface cards in the system is expandable to 24 or to 56 with the use of the HP 2151A I/O Extender or the multiplexed I/O option, respectively. Interface cards and cables necessary for a complete hook-up of each I/O device are provided by respective HP interface kits. Interface kits and I/O devices are ordered separately.

2.5 COMPUTER SYSTEM INPUT/OUTPUT OPERATIONS.

2-6. GENERAL.

2-7. Figure 2-2 illustrates the main elements of the computer system concerned with the control of input/output operations. All elements shown are contained in the computer mainframe except for the external devices. Although the R-, S-, and T-buses are represented as single lines in figure 2-2, each bus is actually 16 individual lines. Also, interface arrangements are shown for only two external devices, one input and one output, where as many as seven devices may be used with the standard model and

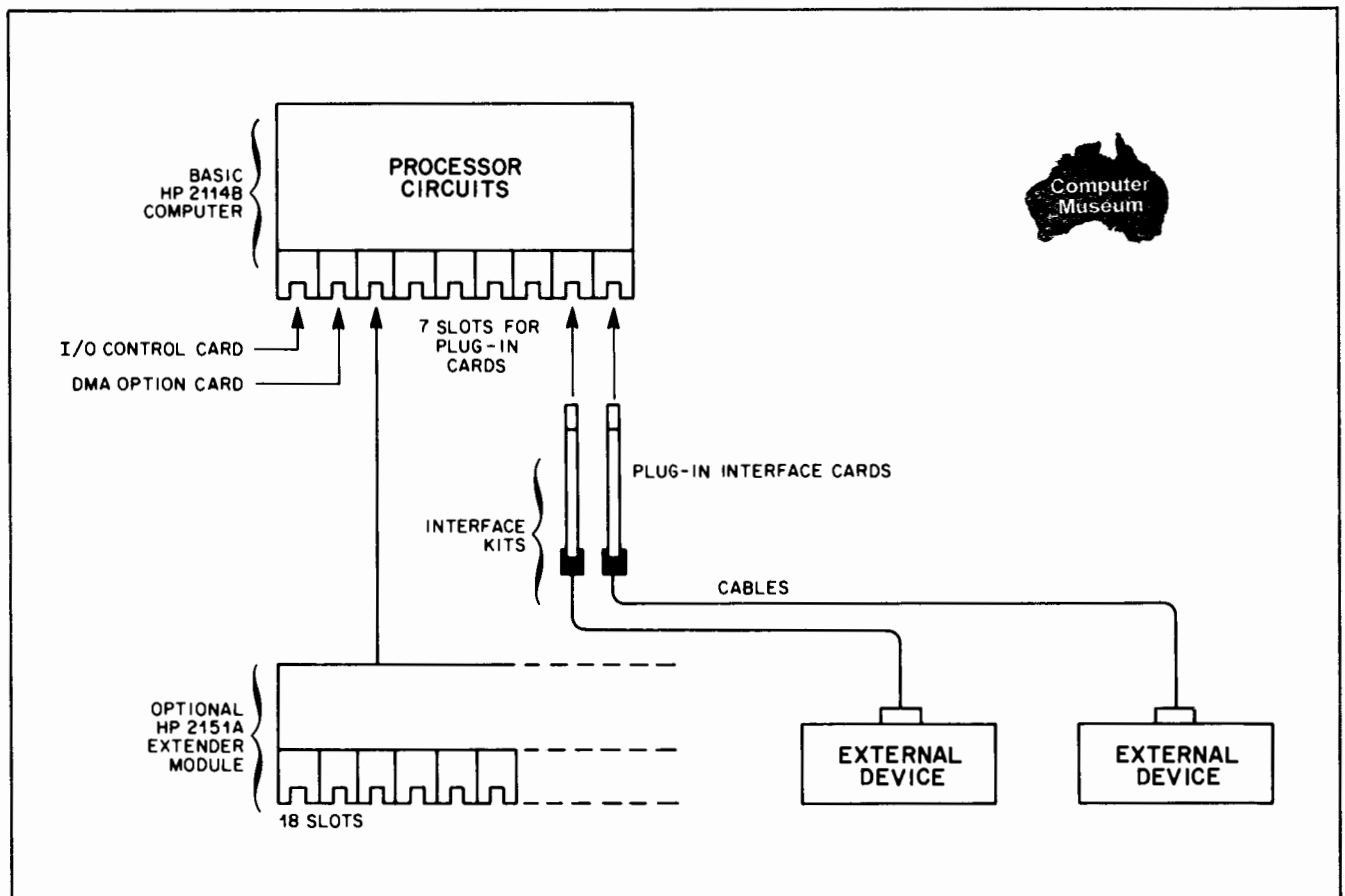


Figure 2-1. Input/Output Structure

up to 56 with the multiplexed I/O option. The elements illustrated process all input/output operations in two ways, as follows:

- a. Process input/output instructions from the computer.
- b. Process interrupt requests from the external devices.

2-8. INPUT/OUTPUT INSTRUCTIONS.

2-9. Input/output instructions from memory via the T-register are first decoded by the I-register and applied to various register gates as input signals (refer to figure 2-2). These decoded instructions are also applied to the I/O control and address logic (on the I/O control card) where they are translated into appropriate control and flag signals. The control and flag signals are routed to various interface cards as determined by the select code (from the T-register via the I/O address logic). The control and flag signals can be used to set or clear the control and flag FF's (flip-flops) on the interface cards, and test their set and clear conditions. Each interface card slot has been permanently assigned to an individual select code through computer wiring. This allows the select code from the T-register to individually address each interface card, and its respective I/O device, on a priority basis.

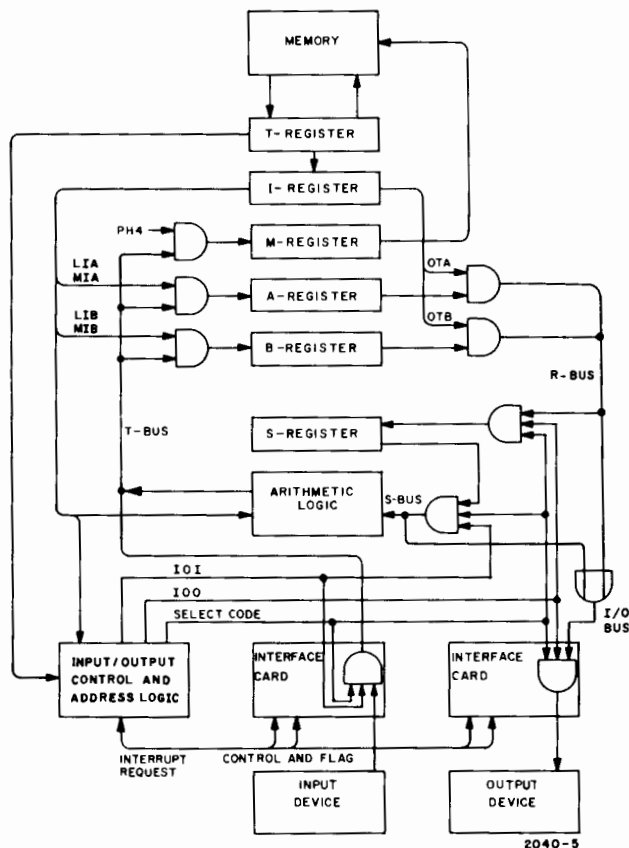


Figure 2-2. Block Diagram of Input/Output System Operation

2-10. The IOI (I/O input) signal strobes all interface cards for input data as a result of a load into A (LIA), load into B (LIB), merge into A (MIA), or a merge into B (MIB) instruction. Only the data from the interface card addressed by the select code can be enabled. The data is strobed by the IOI signal onto the T-bus. From there it is transferred via the arithmetic logic (to alter or combine the data) to the A- or B-register. The particular register which will receive the data is determined by the LIA/B or MIA/B signal present at the register input gate.

2-11. The IOO (I/O output) signal, which is the result of an OTA (output from A) or an OTB (output from B) instruction, is also applied to the interface cards. This signal, when combined with the select code from the T-register, strobes data from the R-bus into the appropriate interface card and I/O device. (Data had previously been placed on the R-bus from the A- or B-register as a result of the OTA or OTB instruction.)

2-12. INTERRUPT REQUESTS.

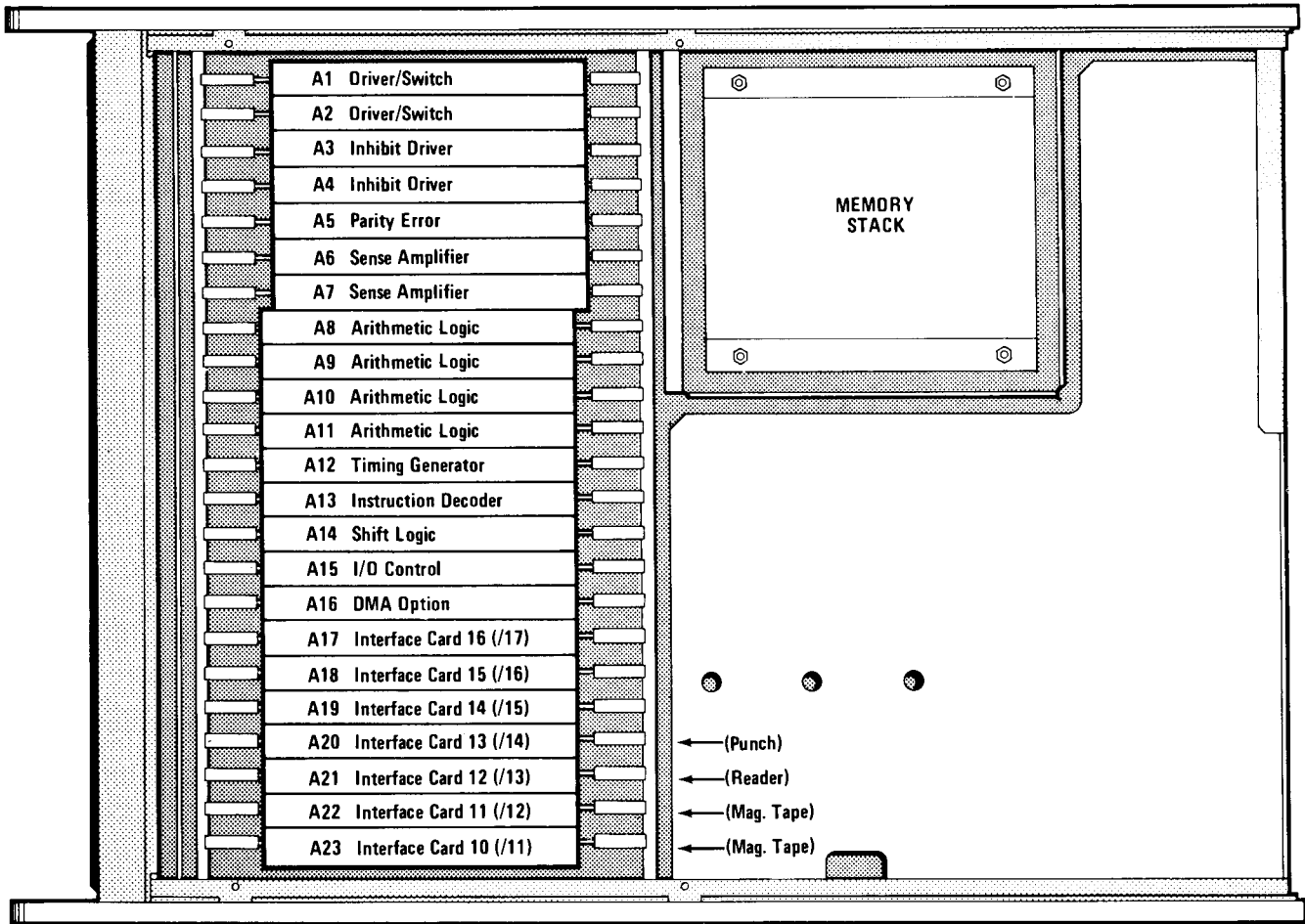
2-13. If a specific instruction to the I/O control card has at some previous time enabled the interrupt system, an external device may then request an interrupt to the computer program at any time. To request an interrupt, an external device applies an interrupt request signal, via the interface card, to the I/O control card (figure 3-3). The I/O control card determines the address of the interrupting device and causes an interrupt of the main computer program. This is done by forcing the M-register to be set (via the T-bus) to a memory location corresponding to the address, or select code, of the interrupting device. This occurs during phase 4, the interrupt machine cycle of computer operation. Following phase 4, the fetch phase is set and the computer executes the instruction contained in the memory location that corresponds to the count held by the M-register. Generally, this will be a jump to a service subroutine (JSB) instruction. The subroutine will prepare and/or accept input data from the external device or apply output data from the computer to the external device. Upon completion of service, the subroutine causes a return to the proper location in the main computer program. Refer to paragraphs 2-26 through 2-50 for a detailed description of the interrupt system.

2-14. INPUT/OUTPUT SYSTEM CARDS.

2-15. I/O CONTROL CARD.

CAUTION

The 48-pin connector of the I/O control card is for use with the I/O extender or multiplex options only. Damage to the computer may result if the connector is connected to any other option or device.



2040-2

Figure 2-3. Plug-In Card Locations (Top View)

2-16. The computer contains one plug-in I/O control card. This card plugs into the computer, adjacent to the interface cards as shown in figure 2-3. The card has built-in extractor handles to aid in its removal from the computer. The I/O control card is connected in parallel with each of the interface cards in the computer and contains the I/O control circuits, I/O address circuits and master interrupt enable flip-flop. The I/O control circuits receive command and timing signals from the computer for transfer to the interface cards. These circuits also provide the flip-flops and gating functions necessary for proper control of interface operation. The I/O address circuits provide a decoding function for program selection of the desired interface card and an encoding function for interface card interrupt identification. For detailed information on the I/O control card, refer to section III of this manual.

2-17. INTERFACE CARDS.

2-18. PURPOSE. The interface cards provide channels through which data is transferred between the computer and the input/output devices, and provide control (via computer commands) of the input/output device operation. An interface card contains flip-flops for temporary storage

of data that is transferred to or from the computer. The number of buffer flip-flops on a particular interface card depends on the type of device connected to it. Other logic circuitry on the interface card also depends on the device to which it is connected. Certain devices are capable of interrupting the computer program, while for others this capability is not necessary; certain devices require control signals for movement of tape while others do not, and timing requirements for some devices must be provided on the interface card. In some cases more than one interface card is required for an external device. Interface cards are provided as part of each interface kit ordered. For detailed information on a particular interface card, refer to the applicable interface kit manual, which is also included in each interface kit.

2-19. LOGIC ELEMENTS. Logic elements on the interface cards are provided by microcircuit packages which may contain more than one logic element and which are in numbered locations on the interface cards. The microcircuit package reference designations on the logic diagrams are preceded by MC. The number following MC corresponds to the numbered location of the package on the particular interface card. The individual elements of a package are

Table 2-1. Interface Card-to-Computer Pin Connections

PIN	SIGNAL MNEMONIC AND DEFINITION	PIN	SIGNAL MNEMONIC AND DEFINITION
1	GND: Ground	2	GND: Ground
3	PRL: Priority Low	4	FLGL: Flag signal, Lower Select Code
5	SFC: Skip Flag Clear (Skip next instruction if Flag FF is reset)	6	IRQL: Interrupt Request, Lower Select Code
7	CLF: Clear (reset) Flag FF	8	IEN: Interrupt Enable
9	STF: Set Flag FF	10	IAK: Interrupt Acknowledge
11	T3IO: Machine phase time T3 to I/O	12	SKF: Skip Flag (Skip next instruction if SFS or SFC test is true)
13	CRS: Control Reset	14	SCM: Select Code Most Significant Digit (Lower Address)
15	IOG: I/O Group instruction	16	SCL: Select Code Least Significant Digit (Lower Address)
17	POPIO: Power On Pulse I/O	18	IOBI16: I/O Bus Input, Bit 16
19	SRQ: Service Request	20	IOO: I/O Output instruction
21	CLC: Clear (reset) Control FF	22	STC: Set Control FF
23	PRH: Priority High	24	IOI: I/O Input instruction
25	SFS: Skip Flag Set (Skip next instruction if Flag FF is set)	26	IOBI0: I/O Bus Input, Bit 0
27	IOBI8: I/O Bus Input, Bit 8	28	IOBI9: I/O Bus Input, Bit 9
29	IOBI1: I/O Bus Input, Bit 1	30	IOBI2: I/O Input, Bit 2
31	IOBI10: I/O Bus Input, Bit 10	32	SIR: Set Interrupt Request
33	IRQH: Interrupt Request, Higher Select Code	34	SCL: Select Code Least Significant Digit (Higher Address)
35	IOBO0: I/O Bus Output, Bit 0	36	+30 volts, unregulated
37	SCM: Select Code Most Significant Digit (Higher Address)	38	IOBO1: I/O Bus Output, Bit 1
39	+4.5 volts	40	+4.5 volts
41	IOBO2: I/O Bus Output, Bit 2	42	IOBO4: I/O Bus Output, Bit 4
43	+12 volts	44	+12 volts
45	IOBO3: I/O Bus Output, Bit 3	46	ENF: Enable Flag
47	-2 volts	48	-2 volts
49	FLGH: Flag Signal, Higher Select Code	50	RUN
51	IOBO5: I/O Bus Output, Bit 5	52	IOBO7: I/O Bus Output, Bit 7
53	IOBO6: I/O Bus Output, Bit 6	54	IOBO8: I/O Bus Output, Bit 8
55	IOBO11: I/O Bus Output, Bit 11	56	IOBO9: I/O Bus Output, Bit 9
57	IOBO12: I/O Bus Output, Bit 12	58	IOBO10: I/O Bus Output, Bit 10
59	(Not Used)	60	IOBO11: I/O Bus Output, Bit 11
61	IOBO13: I/O Bus Output, Bit 13	62	(Not Used)
63	(Not Used)	64	IOBI3: I/O Bus Input, Bit 3
65	IOBO14: I/O Bus Output, Bit 14	66	(Not Used)
67	(Not Used)	68	(Not Used)
69	-12 volts	70	-12 volts
71	(Not Used)	72	(Not Used)
73	(Not Used)	74	IOB15: I/O Bus Output, Bit 15
75	(Not Used)	76	(Not Used)
77	IOBI4: I/O Bus Input, Bit 4	78	IOBI12: I/O Bus Input, Bit 12
79	IOBI13: I/O Bus Input, Bit 13	80	IOBI5: I/O Bus Input, Bit 5
81	IOBI6: I/O Bus Input, Bit 6	82	IOBI14: I/O Bus Input, Bit 15
83	IOBI15: I/O Bus Input, Bit 15	84	IOBI7: I/O Bus Input, Bit 7
85	GND: Ground	86	GND: Ground

NOTE: Pins 1 & 2, 39 & 40, 43 & 44, 47 & 48, 69 & 70, and 85 & 86 connected together on slot connector and on interface card.

further identified by a suffix letter. For example, the reference designation MC86A refers to logic element A within the microcircuit package at location 86 on the interface card. Refer to the appendix in the installation and maintenance manual, volume two for logic diagrams for each of the microcircuit packages according to HP part number.

2-20. PIN ASSIGNMENTS. Refer to figure 2-4. One end of each interface card has 86 printed-circuit paths, 43 on each side of the card. This end of the card plugs into a computer slot connector to transfer signals to and from the computer. It is also keyed to prevent incorrect insertion. The circuit path positions correspond to the pin positions of the slot connector. Odd-numbered pins 1 through 85 are on one side of the card as shown in figure 2-4, and even-numbered pins 2 through 86 are on the other side of the card. Pins 1 and 2 are directly opposite each other on the card. Pin assignments for this end of the card are identical for all interface cards to permit the placement of any card in any of the input/output slots of the computer.

2-21. The other end of the interface card has 48 printed-circuit paths, 24 on each side of the card. The plug connector of the interconnecting cable to the input/output device plugs onto this end of the card to transfer signals to and from the device. The circuit-path positions correspond to the pin positions of the plug connector. Pins 1 through 24 are on one side of the card as shown in figure 2-4, and consecutively-lettered pins A through BB (with letters G, I, O and Q intentionally omitted) are on the other side of the card. Pins 1 and A are directly opposite each other on the card. Also on this end of the card are two extractor handles to aid in the removal of the card from the computer slot.

2-22. Refer to table 2-1 for a list of the pin connections and signals between the interface cards and the slot connectors. Although this table lists all of the pin assignments and signals between the cards and the slot connectors, an individual interface card may not necessarily use all signals. Pin assignments and signals between an interface card and its input/output device is provided in each interface kit manual.

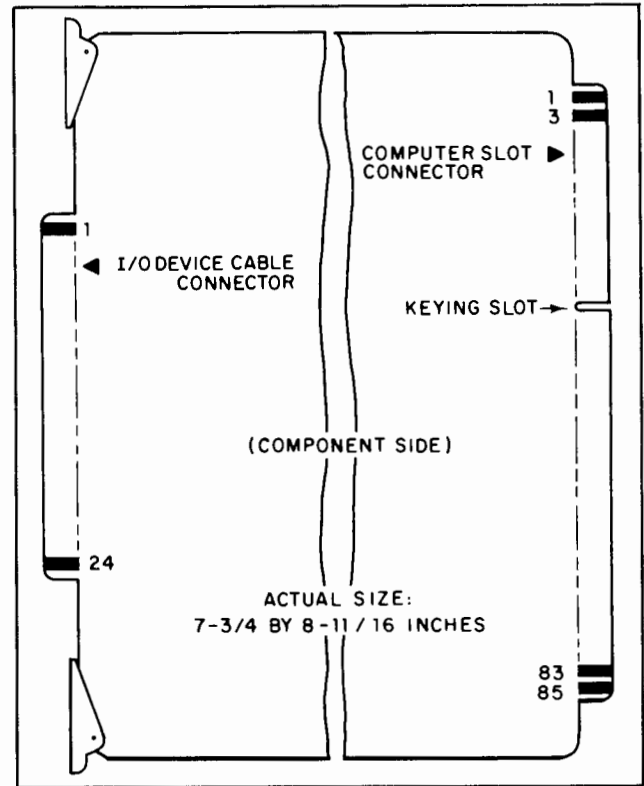


Figure 2-4. Interface Card Connectors

2-23. INPUT/OUTPUT DEVICE SELECTION.

2-24. Bits 0 through 5 of the input/output instruction form a select code to specify one of 64 possible input/output devices or functions. The select code is applied to the address circuits located on the I/O control card. These circuits decode the 6-bit code and provide a two-digit octal code output. This output is transferred to the interface-card slot of the selected input/output device to permit program control of the device. Table 2-2 lists the select codes and their assignments, and indicates the corresponding interrupt location (i.e., the memory location containing the instruction to be executed when an interrupt occurs). Select code 00 gives access to the master interrupt system enable flip-

Table 2-2. Select Code Assignments

SELECT CODE (OCTAL)	INTERRUPT LOCATION	ASSIGNMENT
00	None	Interrupt System Enable Disable
01	None	Switch Register or Overflow
02	00002	Direct Memory Access Option
03	None	Not Assigned
04	00004	Power Fail Interrupt/Central Interrupt Register
05	00005	Parity Error Interrupt
06	00006	Direct Memory Access Option
07	00007	Not Assigned
10	00010	I/O Device, Highest Priority
thru	thru	thru
77	00077	I/O Device, Lowest Priority

flop on the I/O control card. Select code 01 allows access to either the overflow or switch registers. Codes 02 through 07 are reserved for processor input/output functions or options, as listed. Codes 10 through 77 (octal) are used for selection of 56 possible input/output devices (with the multiplexed I/O option installed), each capable of causing an interrupt.

2-25. Figure 2-3 illustrates the slots in the computer for the plug-in cards associated with input/output operation. Each of the interface-card slots actually has two select codes assigned to it. This provides for I/O devices which contain both input and output logic circuits (e.g., magnetic tape input/output in positions 22 and 23 of figure 2-3). The input portion and the output portion of the card may require separate select codes. When an interface card contains addressable input and output logic on the same card (position 23 in figure 2-3) the slot connector must provide both select codes to a single I/O slot. The second interface card maintains priority continuity as described in paragraph 2-43. Since the slot connector wiring determines the select codes of the slots and interface cards can be plugged into any slot, the interface card assumes the select codes of the slot it is plugged into. (Interface cards are assigned to particular slot positions before shipment of a computer system and may vary from system to system. The slot positions of the interface cards in figure 2-3 are for illustration purposes only.)

2-26. INTERRUPT SYSTEM.

2-27. The interrupt system provides the means for an

external device to interrupt the program in progress when data is available or when additional output data can be accepted. Figure 2-5 illustrates the relationship between the computer, the I/O control card, and typical interrupt logic on a particular interface card. (Figure 2-5 is for interrupt-logic explanatory purposes only.) Refer to figure 2-6 for a chart of typical interrupt system timing.

2-28. An interrupt request from an external device occurs when the following conditions are met:

- a. The interrupt system is enabled.
- b. The flag flip-flop of the specific device interface card is set.
- c. The control flip-flop of the specific device interface card is set.
- d. No priority-affecting instruction (STF, CLF, STC or CLC) is in progress.
- e. No higher-priority devices satisfy the conditions "a" through "d".

2-29. INTERRUPT SYSTEM ENABLE/DISABLE.

2-30. The computer program determines if interrupt requests from the external devices will be recognized. This is accomplished by enabling or disabling the interrupt system enable flip-flop on the I/O control card. A set flag (STF) instruction with a select code of 00 (octal) sets the

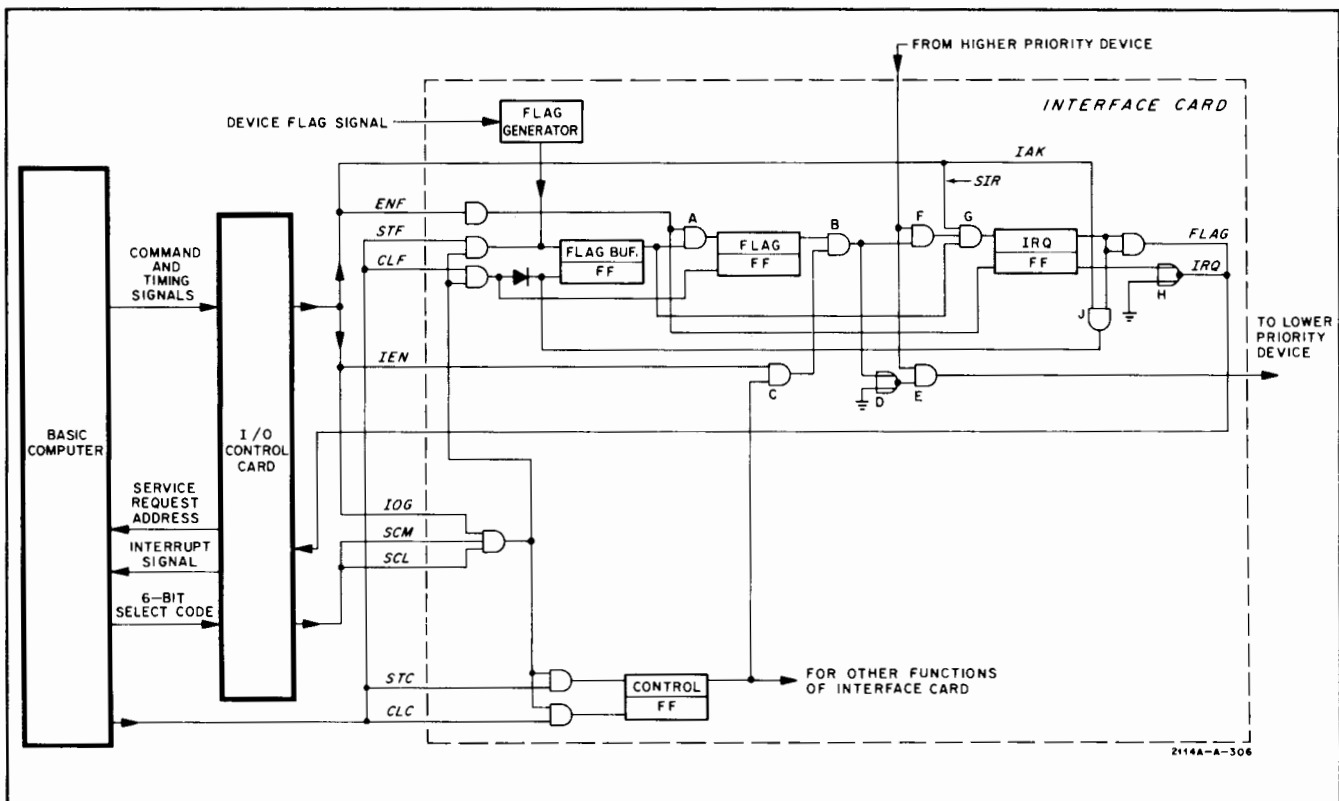


Figure 2-5. Typical Interrupt Logic

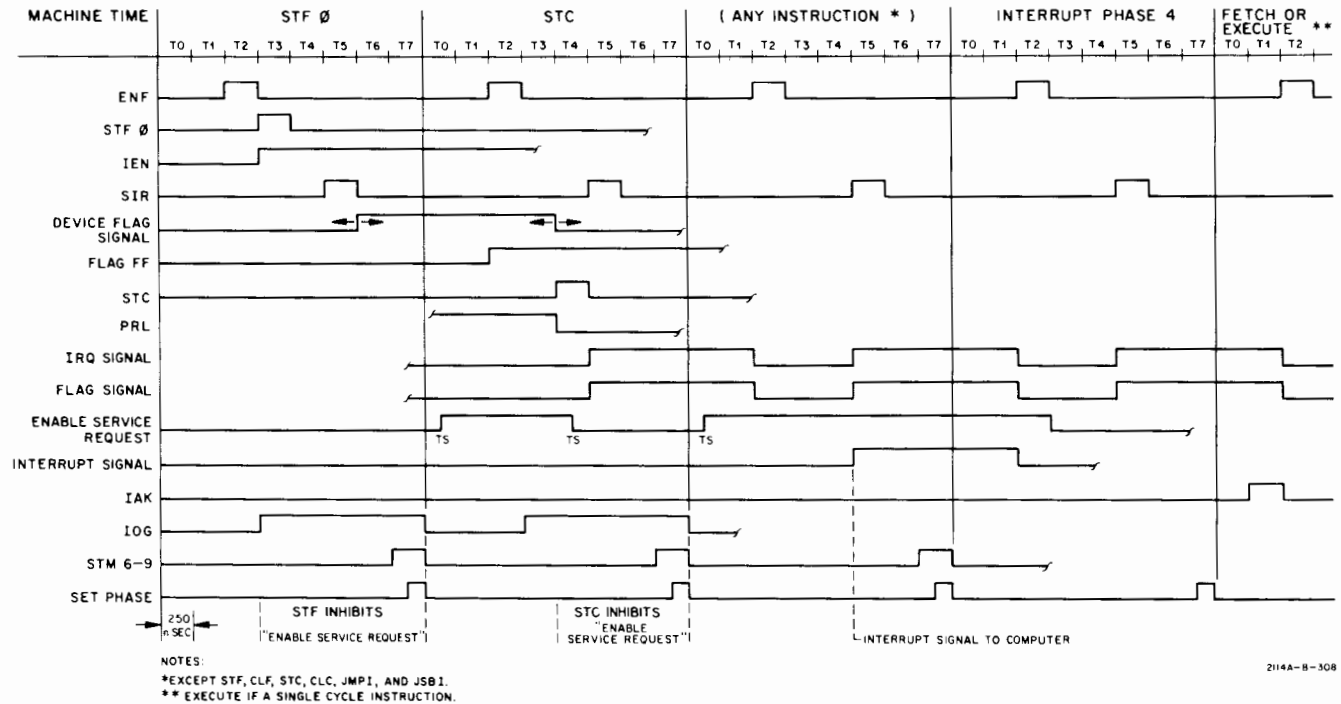


Figure 2-6. Typical Interrupt System Timing

flip-flop and enables the interrupt system. A clear flag (CLF) instruction with a select code of 00 (octal) clears the flip-flop and disables the interrupt system.

2-31. When computer power is initially turned on, the interrupt system enable flip-flop is automatically cleared, disabling the interrupt system. Initial turn-on also clears all control flip-flops on the interface cards to prevent input/output devices from running when power is applied, and sets all flag buffer and flag flip-flops on the interface cards. Therefore, to operate any device under interrupt system control it is first necessary to set the interrupt system enable flip-flop, clear the individual flag buffer and flag flip-flops, and set the individual control flip-flop.

2-32. INTERRUPT SYSTEM OPERATION.

2-33. When the external device has completed its operation, it generates a device flag signal to the interface card flag generator which sets the flag buffer flip-flop (see figure 2-5). The output of the flag buffer flip-flop in conjunction with the ENF (enable flag) signal from the I/O control card at time T2 (figure 2-6) causes "and" gate A to set the flag flip-flop. The flag flip-flop output is "anded" at gate B with the output of "and" gate C. The gate C output is true when the control flip-flop is set and when the IEN (interrupt enable) signal is received from the I/O control card at time T3. Unless the control flip-flop is set by a set control (STC) instruction, an interrupt request cannot occur.

2-34. The control flip-flop is set under program control and therefore, may be set at any T4 time of a machine cycle, depending on the type of operation being performed.

The STC instruction is enabled to the control flip-flop by the SCM (select code most significant digit) and SCL (select code least significant digit) signals and the IOG (I/O group instruction) signal from the I/O control card. The SCM and SCL signals are enabled on the individual interface card by the IOG signal which occurs when the instruction to be performed is an I/O group instruction. When the control flip-flop sets, a true input is applied to "and" gate C. The inputs to "and" gates B and C are then true and gate B applies a true output to inverting "or" gate D. The false output of gate D disables "and" gate E, making the priority network bus to the lower-priority devices false. This prevents any device of lower priority from requesting an interrupt.

2-35. At the same time that gate B applied a true output to gate D, it also applied a true output to "and" gate F. The priority network signal to gate F will be true if an interface card (device) of higher priority than the one represented in figure 2-5 is not requesting an interrupt. In this case, the true output of gate F is combined with the SIR (Set Interrupt Request) signal from the I/O control card at time T5 and the output of the set flag buffer flip-flop to provide a true output from "and" gate G. The gate G output sets the IRQ (interrupt request) flip-flop.

2-36. The IRQ flip-flop outputs provide the flag signal and the IRQ signal to the I/O address circuits. (The IRQ signal is obtained by the inversion of the false clear side output of the IRQ flip-flop by inverting "or" gate H.) The flag signal is "anded" in the I/O address circuits with the enable service request (ESR) signal from the I/O control circuits to form an interrupt signal. However, the ESR

signal is false for the remainder of the machine cycle during which an instruction occurs that effects device priorities (STC in figure 2-6) as determined by the I/O control circuits. At time T2, the IRQ flip-flop is cleared by the ENF signal to allow a higher-priority device to request an interrupt. If the control flip-flop is still set and no higher-priority devices have requested an interrupt, the IRQ flip-flop will again be set at time T5 (SIR). The flag and IRQ signals are again sent to the I/O address circuits. The signals are used to form a 6-bit service request address to be sent to the computer at time T7 of the interrupt phase 4. The flag signal and the now true ESR signal form the interrupt signal which is sent to the computer. This signal causes an interrupt at the end of the current machine phase, switching the computer into the interrupt phase, except when any of the following conditions occur:

a. The computer is in the halt mode.

b. A jump indirect (JMP,I) or a jump to subroutine indirect (JSB,I) instruction is not fully executed. (These instructions inhibit all interrupts until fully executed for any number of indirect levels of addressing. An interrupt request will be granted at the beginning of the machine phase immediately following the complete execution of the JMP,I or JSB,I instruction.)

2-37. INTERRUPT PROCESSING.

2-38. During interrupt phase 4, the computer decrements the P-register by one to ensure that the proper location in the main program will be returned to after the interrupt is processed. (The P-register was incremented by one at time T7 of the last machine phase of the main program by the STM6-9 signal.) Also, the computer places the service request address (which is always equal to the select code of the interrupting device) from the I/O address circuits into the M-register at time T7. This causes the next instruction to be read from the memory location having the same number as the service request address (select code) during the fetch phase (phase 1). This location in memory is referred to as the "interrupt location" and is reserved for that particular device. For example, a device specified by a select code of 10 will interrupt to (i.e., causes execution of the contents of) memory location 00010. At time T3 of phase 4, the interrupt system is inhibited by the false enable service request signal until the fetch phase following the execution of the instruction at the interrupt location. This prevents interrupts from occurring until at least one fetch phase has been executed.

2-39. At time T1 of fetch phase (phase 1) the IAK (interrupt acknowledge) signal from the I/O control card and the set-side output of the IRQ flip-flop clears the flag buffer flip-flop through "and" gate J (figure 2-5). Since the set-side output of the flag buffer flip-flop is applied to "and" gate G, clearing the flip-flop prevents the setting of the IRQ flip-flop which would cause another interrupt from the same flag signal at time T5 of phase 1 when the SIR signal is again applied to gate G. (The flag buffer flip-flop can also be cleared by a programmed CLF (clear flag) instruc-

tion.) At time T2, the ENF signal clears the IRQ flip-flop. The computer fetches the instruction in the interrupt location which will usually be a jump to a subroutine (JSB,I) instruction, although any legal instruction may be placed in the interrupt location. The contents of the P-register plus one are stored in the first location (X) of the subroutine. (Since the previous contents of the first memory location are destroyed when P + 1 is stored, the first instruction of the subroutine should always be a no-operation (NOP) instruction or equivalent.) The location of the subroutine (X + 1) is placed in the P- and M-registers, and the computer resumes operation in the subroutine. Thus, the instruction at location X + 1 is the first instruction of the subroutine to be executed. The contents of the working registers that were in use in the main program should be stored when entering the subroutine and restored before exit from the subroutine. The exit from the subroutine is made with a JMP,I to location X. This places the address of the interrupted program instruction in the P- and M-registers and normal program operation resumes.

2-40. INTERRUPT PRIORITY.

2-41. PRIORITY ASSIGNMENTS. A priority network on the interface cards allow only one external device to interrupt the computer program regardless of the number of devices requesting an interrupt. The priority network gives highest priority to select code 04, reserved for power failure interrupt option 08, and decreasing priority to select codes in order from 05 through 77 (see table 2-2).

2-42. As shown in figure 2-3, each of the interface card slots in the computer is assigned two interrupt priorities corresponding to the two select codes assigned each slot. This provides an interrupt priority for both the input and output portions of an interface card, if they are separately addressable. The interrupt priority assignments of each slot remain fixed but since any interface card can be plugged into any slot, the interrupt priority of a given device can be easily changed by plugging the device interface card into another slot.

2-43. PRIORITY NETWORK OPERATION' As shown in figure 2-7, priority is established by a hardware-implemented priority chain. The true-false logic levels for an interface card which is not requesting an interrupt are illustrated on the first interface card (select code 10) with the interrupt system enabled (IEN input is true). Also, the PRH (Priority high) signal is true, indicating that a device of higher priority is not requesting an interrupt. In this case, the "chain" is not broken and a true PRL (priority low) signal is available to the next interface card (select code 11) as a true PRH signal to that card.

2-44. When the interface card contains both input and output logic, each type of logic may have a separate select code and corresponding interrupt priority, with the priority chain connected internally. The output logic of the interface card is usually of higher priority than the input logic on cards containing both types of logic. Since this interface card uses both select codes assigned to its slot, the second

interface card for the I/O device (for an example see the magnetic tape interface cards in figure 2-3) must provide continuity for the priority network. There can be no gaps in the network for it to function properly.

2-45. If the output logic portion of the interface card requests an interrupt, the PRL signal to the input logic portion of the interface card is then false, breaking the "chain", and preventing any interface card of lower priority from interrupting the computer program. A service subroutine can then be entered to process the interrupt of the output logic.

2-46. A service subroutine of any device can be interrupted by a higher priority device; then after the higher priority interrupt subroutine is completed, the lower priority subroutine may continue. In this way, several service subroutines may be in a state of interruption at one time. Each will be permitted to continue when the next higher priority subroutine is completed.

2-47. Interrupt priority can also be program controlled. Since an interrupt cannot occur unless the control flip-flop of the interface card is set, all control flip-flops on the interface cards of higher priority than the one desired can be cleared by a clear control (CLC) instruction. This prevents those interface cards from requesting an interrupt and

establishes the desired device as the highest-priority device. However, these devices must then be serviced by testing the flag and/or setting the control flip-flop again.

2-48. INTERRUPT PRIORITY CONTINUITY.

2-49. Figure 2-7 illustrates the continuity of the interrupt priority network for input/output interface cards plugged into the computer mainframe or into an I/O extender. The interrupt system enable flip-flop shown in figure 2-7 is located on the I/O control card.

2-50. Since the power failure interrupt option (select code 04) is on at all times, it can interrupt the computer regardless of the state of the interrupt system enable flip-flop. For all other interface cards and options, (with the exception of the memory parity check option) the flip-flop must be set before an interrupt can occur. When an interface card requests an interrupt, its false PRL signal is applied to the next interface card as a false PRH signal to prevent it from requesting an interrupt. This sequence continues from card to card until the last interface card receives a false PRH signal.

2-51. EXTENDER MODULE.

2-52. An HP 2151A Extender must be used when more

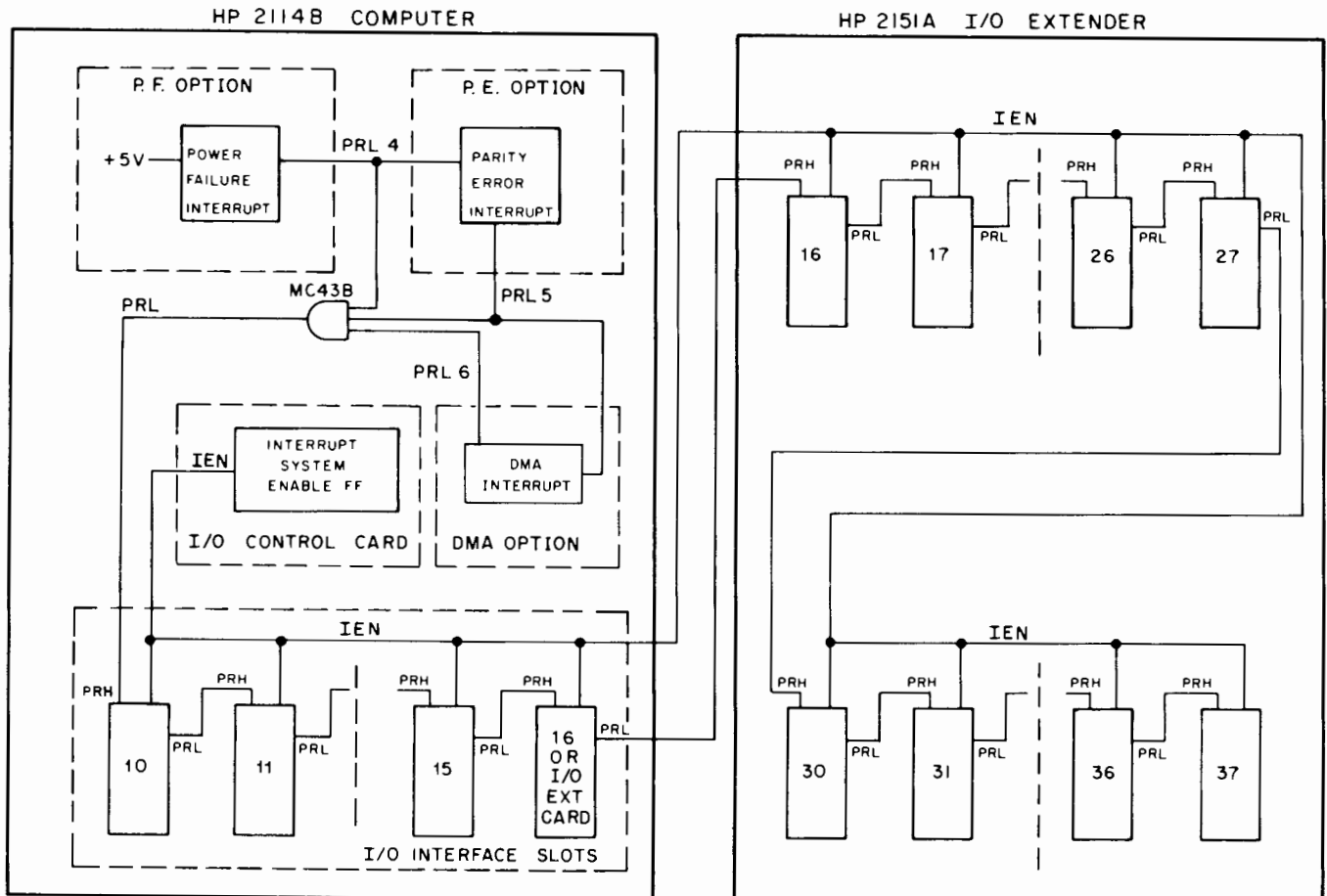


Figure 2-7. Priority Continuity

2040-3

than seven interface cards are required for the computer system. This extender is a separate rack-mount unit which may also be used freestanding. It has its own self-contained power supply. Up to 18 interface cards may be plugged into the HP 2151A. Since the extender requires one I/O slot in the computer mainframe there is a total of 24 I/O slots available, six in the mainframe and 18 in the extender.

Table 2-3. Current Available for I/O Options

	+30V	+12V	-12V	-2V	+5V
Current Available from HP 2114B Computer Supply	0.1A	1.5A	1.5A	4A	15A

2-53. POWER SUPPLY.

2-54. The computer's internal power supply is adequate

for a full complement of seven plug-in options. When additional I/O devices are used with the HP 2151A Extender these units (up to 18) are powered by the extender's power supply.

2-55. Table 2-3 lists the current available from the HP 2114B Computer power supply.

2-56. INTERFACE KITS.

2-57. Interface kits for the HP 2114B Computer system provide the necessary interface cards and cables for connection of external equipment to the computer. The necessary software for driving the specific peripheral device and device diagnostic program tapes are also provided. The kits are identified by a 5-digit accessory number, a suffix revision letter and a functional name (e.g., 12531B Buffered Teleprinter Input/Output). Software tapes are identified by their name and HP accessory number on both the tape container and the tape itself.

SECTION III

I/O CONTROL CARD



3-1. INTRODUCTION.

3-2. This section provides theory of operation information for the I/O control card (part no. 02114-6007). The card is of standard interface card size and plugs into position 15 in the card slots. The slot connector transfers signals to and from the card (see table 3-1). Additional cabling from the 48-pin connector at the top of the card is required only if an I/O extender or multiplexed I/O option is used. The 48-pin connector provides additional control and addressing information for the added I/O devices (see table 3-2). The card output signals are transferred to all interface cards in the computer through the interface-card slot connectors. The main functions of the I/O control card are control of the interrupt system, decoding of select codes and the encoding of flag and IRQ signals. The decoding of the 6-bit code from the computer provides the 2-digit octal select code for selection of the interface card through which the computer is to communicate with the input/output device. The encoding of the flag and IRQ signals from the interface cards provides a 6-bit address and an interrupt signal to the computer. The 6-bit address identifies the interface card (device) requesting an interrupt. Certain clock signals, reset signals, and selection of the switch and overflow registers are also provided by the I/O control card.

CAUTION

The 48-pin connector of the I/O control card is for use with the I/O extender or multiplex options only. Damage to the computer may result if the connector is connected to any other option or device.

3-3. THEORY OF OPERATION.

3-4. COMPUTER POWER-ON.

3-5. When power is initially applied by turning on the POWER switch behind the computer front panel, the computer is preset to time T5 of the fetch phase (phase 1). At this time, the POPIO signal (figure 3-3) is received at pin 17 of the I/O control card. This signal is present for 100 milliseconds. (With power on, pressing the PRESET switch applies the POPIO signal to the control card for as long as the switch is pressed.) During the presence of the POPIO signal the computer clock runs and continually repeats times T0 through T7 while remaining in phase 1. When the POPIO signal drops, the computer is in phase 1 and the initial conditions of the interface cards have been established for proper operation. The POPIO signal performs the following functions which are described in paragraphs 3-6 through 3-9:

- a. Disables the interrupt system.
- b. Provides a false enable service request (ESR) signal.
- c. Sets the flag buffer and flag flip-flops and clears the IRQ flip-flop on all interface cards.
- d. Clears the control flip-flop on all interface cards.

3-6. The POPIO signal clears the interrupt system enable flip-flop through gates MC25A and MC44D disabling the interrupt system.

3-7. When the interrupt system enable flip-flop is cleared, the false output of the flip-flop is applied to the input of "and" gate MC95A. The output of gate MC95A is now a false ESR signal. This prevents an interrupt signal from being sent to the computer which would switch the computer into interrupt phase 4.

3-8. The POPIO signal directly sets the flag buffer flip-flop on all interface cards. At time T2, the T2 clock signal clears the IRQ flip-flop and together with the set flag buffer flip-flop output, sets the flag flip-flop on all interface cards.

3-9. The POPIO signal forms the CRS signal through "and" gate MC25A, to set the flag buffer flip-flop on all interface cards and to clear the interrupt control flip-flop (MC35B) through "nand" gate MC23B on the I/O control card. (The CRS signal can also be programmed by a CLC instruction with a select code of 00 (octal); see paragraph 3-20.) Clearing the control flip-flop MC35B ensures a false enable service request signal when the POPIO signal drops. This prevents an interrupt from occurring until after time T7 of the first machine phase after the POPIO signal drops to permit the execution of at least one program instruction. (The clear-side output of the interrupt control flip-flop enables "and" gate MC36C at time T1 of phase 1 which enables "and" gate MC26B to form the IAK signal. The IAK signal has no effect on the interface cards during the presence of the POPIO signal.)

3-10. SIR SIGNAL.

3-11. At each T5 clock time, the SIR signal is received by the I/O control card from the computer (figure 3-3). This signal is applied to all interface cards. The SIR (set interrupt request) signal then enables the setting of the IRQ (interrupt request) flip-flop on the interface card to provide flag and IRQ signals to the I/O control card during an interrupt request.

3-12. PRIORITY-AFFECTING INSTRUCTIONS.

3-13. Four instructions, STC, CLC, STF, and CLF, affect the priority structure of the input/output devices. Whether a device can request an interrupt or not depends upon whether its interface-card control flip-flop is set or cleared (STC, CLC) and its flag flip-flop is set or cleared (STF, CLF). If a device cannot request an interrupt, all succeeding lower priority devices assume a priority of one higher in the priority chain, and vice versa.

3-14. The four instructions also inhibit all interrupts during the machine phase in which they occur by removing the enable service request signal to the I/O address circuits. This prevents interrupts during entry and exit from sub-routines. Also, a combination of two of the four instructions are normally the next-to-last instruction in a service subroutine processing an interrupt (the last being a JMP,I instruction to cause return to the main program or to an address in another service subroutine). If another input/output device could interrupt immediately after execution

Table 3-1. I/O Control Card-to-Computer Pin Connections

PIN	SIGNAL MNEMONIC AND DEFINITION	PIN	SIGNAL MNEMONIC AND DEFINITION
1	GND: Ground	2	GND:Ground
3	PON: Power On Pulse	4	FLG 1: Flag 1
5	SFC: Skip Flag Clear (Skip next instruction if Flag FF is reset)	6	\overline{RSP} : "not" Restart Pulse
7	CLF: Clear (reset) Flag FF	8	IEN: Interrupt Enable
9	STF: Set Flag FF	10	IAK: Interrupt Acknowledge
11	T3IO: Machine phase time T3 to I/O	12	SKF: Skip Flag (Skip next instruction if SFS or SFC test is true)
13	CRS: Control Reset	14	IFF: Inhibit Flag Flip-Flop
15	PH1: Machine Phase 1 (Fetch)	16	STM6-9: Store T-Bus in M bits 6-9
17	POPIO: Power On Pulse to I/O	18	T1: Machine phase time T1
19	T0: Machine phase time T0	20	TS: Time period, Second half
21	CLC: Clear (reset) Control FF	22	STC: Set Control FF
23	PRS: Preset Switch	24	PRL4: Priority Low 4
25	SFS: Skip Flag Set (Skip next instruction if Flag FF is set)	26	$\overline{RSM6-9}$: "not" Reset M Register bits 6-9
27	PWF: Power Fail Signal	28	(Not Used)
29	IRQ2: Interrupt Request 2	30	FLG0 (GND)
31	IRQ1: Interrupt Request 1	32	SIR: Set Interrupt Request
33	INT: Interrupt	34	PH4: Machine phase 4
35	FLG2: Flag 2	36	$\overline{TB3}$: "not" T-Bus bit 3
37	IRQ5: Interrupt Request 5	38	IRQ7: Interrupt Request 7
39	+5 volts	40	+5 volts
41	IRQ3: Interrupt Request 3	42	IRQ4: Interrupt Request 4
43	(Not Used)	44	(Not Used)
45	IRQ6: Interrupt Request 6	46	ENF: Enable Flag
47	-2 volts	48	-2 volts
49	$\overline{TB0}$: "not" T-Bus bit 0	50	$\overline{TB1}$: "not" T-Bus bit 1
51	$\overline{TB2}$: "not" T-Bus bit 2	52	$\overline{TB4}$: "not" T-Bus bit 4
53	FLG3: Flag 3	54	$\overline{TB5}$: "not" T-Bus bit 5
55	TR2: T-Register bit 2	56	(Not Used)
57	TR0: T-Register bit 0	58	TR1: T-Register bit 1
59	SCL3: Select Code Least	60	(Not Used)
61	SCL0: Select Code Least significant digit 0	62	SCL4: Select Code Least significant digit 4
63	SCL2: Select Code Least significant digit 2	64	SCL1: Select Code Least significant digit 1
65	SCL6: Select Code Least significant digit 6	66	IOI: I/O Input instruction
67	SCL5: Select Code Least significant digit 5	68	$\overline{SCL7}$: Select Code Least significant digit 7
69	IOG: I/O Group instruction	70	\overline{PINT} : "not" Parity Interrupt
71	PRL6: Priority Low 6	72	SCM2: Select Code Most significant digit 2
73	PRL5: Priority Low 5	74	PRH10: Priority High 10
75	TR5: T-Register bit 5	76	$\overline{PH5}$: "not" Machine Phase 5
77	TR3: T-Register bit 3	78	TR4: T-Register bit 4
79	\overline{HIS} (+5V): "not" Hold Interrupt System	80	SCM1: Select Code Most significant digit 1
81	SCM0: Select Code Most significant digit 0	82	(Not Used)
83	\overline{PEH} : "not" Parity Error Halt	84	SCM3: Select Code Most significant digit 3
85	GND: Ground	86	GND: Ground

Table 3-2. I/O Control Card-to-Extender Pin Connections

PIN	SIGNAL MNEMONIC AND DEFINITION	PIN	SIGNAL MNEMONIC AND DEFINITION
1	GND: Ground	A	(Not Used)
2	FLG1: Flag 1	B	(Not Used)
3	FLG2: Flag 2	C	\overline{XINT} : "not" External Interrupt
4	SCM1: Select Code Most significant digit 1	D	$\overline{IA1}$: "not" Interrupt Address 1
5	$\overline{IA2}$: "not" Interrupt Address 2	E	$\overline{IA0}$: "not" Interrupt Address 0
6	$\overline{IA5}$: "not" Interrupt Address 5	F	$\overline{IA4}$: "not" Interrupt Address 4
7	$\overline{IA3}$: "not" Interrupt Address 3	H	(Not Used)
8	(Not Used)	J	(Not Used)
9	(Not Used)	K	(Not Used)
10	(Not Used)	L	(Not Used)
11	(Not Used)	M	SCM2: Select Code Most significant digit 2
12	(Not Used)	N	SCM3: Select Code Most significant digit 3
13	(Not Used)	P	(Not Used)
14	IRQ1: Interrupt Request 1	R	(Not Used)
15	IRQ2: Interrupt Request 2	S	(Not Used)
16	IRQ3: Interrupt Request 3	T	(Not Used)
17	IRQ4: Interrupt Request 4	U	SCL0: Select Code Least significant digit 0
18	IRQ5: Interrupt Request 5	V	SCL1: Select Code Least significant digit 1
19	IRQ6: Interrupt Request 6	W	SCL2: Select Code Least significant digit 2
20	IRQ7: Interrupt Request 7	X	SCL3: Select Code Least significant digit 3
21	(Not Used)	Y	SCL4: Select Code Least significant digit 4
22	XPF: External Power Fail signal	Z	SCL5: Select Code Least significant digit 5
23	(Not Used)	AA	SCL6: Select Code Least significant digit 6
24	GND: Ground	BB	SCL7: Select Code Least significant digit 7

of these instructions (and before the JMP,I instruction), the possibility would exist that the first device may interrupt a second time before the JMP,I instruction is performed. In this event, the first main-program address (or the other service-subroutine address) stored in the beginning of the service subroutine would be destroyed, preventing a return to the main program or to the other service subroutine.

3-15. Refer to figure 3-3. Whenever any of the four instructions are programmed, the STC, CLC, STF and CLF signals are received by the I/O control card and applied to gates MC23C, MC23D, MC13D, and MC13C, respectively. The applicable gate output is then a "false" input to the inverted clear side of the interrupt control flip-flop (MC35B). The presence of one of the four priority-affecting instructions disables the interrupt system by clearing the interrupt control flip-flop.

3-16. The IOG signal from the computer is sent to the I/O control card and all I/O slots at time T3 of each machine phase that an I/O group instruction is performed and is applied to one input of "and" gate MC95B. The other two inputs are true when the select code 00 (octal) is used. When an I/O group instruction using select code 00 is used, the output of this gate will be true. This provides an enabling signal for gates MC24A, MC25B, MC14A and MC14B.

3-17. The cleared control flip-flop MC35B provides a false set output to MC95A causing a false enable service request

signal. This causes one input of MC85A to go true causing the INT signal to go false. This prevents interrupt signals from being enabled for the remainder of the current machine phase.

3-18. At time T7 of the current machine phase, the STM6-9 signal sets the interrupt inhibit flip-flop MC46C/D. At time T0, TS of the next machine phase MC46A clears the interrupt inhibit flip-flop. The clear side of this flip-flop is applied to the clock terminal of the interrupt control flip-flop MC35B, setting it at T0, TS by the trailing (negative-going) edge of the pulse output of the interrupt inhibit flip-flop. The true set side output of the interrupt control flip-flop MC35B enables MC95A providing a true enable service request signal which enables interrupt signals to the computer.

3-19. CLEARING CONTROL FLIP-FLOPS.

3-20. The control flip-flop on all interface cards can be cleared by the CLC instruction with a select code of 00. The CLC signal enters the I/O control card at pin 21 and is applied to one input of "and" gate MC25B. The other input to MC25B is made up of select code 00 and the IOG signal which are "anded" together at MC95B to form the address 00 signal. The output of MC25B is true when the CLC instruction is used with a select code of 00. This true output generates a true CRS signal which clears the control flip-flop on the interface cards to prevent an interrupt request from any I/O device.

3-21. PHASE OPERATION.

3-22. INTERRUPT PHASE 4. During phase 4, the PH4 signal and clock signal T3IO are received by the I/O control card on pins 34 and 11 respectively. T3IO, a buffered T3 signal, is also applied to all interface card slots. On the I/O control card these signals are "nanded" by MC13B. When phase 4, T3 is true both inputs to MC13B will be true giving a false output. This output clears the interrupt control flip-flop MC35B. The false set-side output of MC35B disables MC95A. The output of MC95A goes false removing the enable service request signal. Interrupt signals will not now be enabled to the computer until after the program counter steps (time T7 of fetch phase 1).

3-23. FETCH PHASE 1. At time T1 of fetch phase 1, directly following the interrupt phase, the PH1 signal and clock signal T1 are applied to "and" gate MC36C. The true clear-side of the interrupt control flip-flop forms the third input to MC36C. The true output of MC36C provides an IAK signal to all interface-card slot connectors. The IAK signal causes the flag buffer flip-flop on the interface card which initiated the interrupt to be cleared.

3-24. The enable service request signal is inhibited during interrupt phase 4 until after time T7 of the fetch phase of the instruction in the computer memory interrupt location unless further disabled by a JMP,I or JSB,I instruction in the interrupt location. This ensures full execution of at least one cycle before interrupts are again enabled. At time T7 of the fetch phase, the STM6-9 signal enters the I/O control card at pin 16 and is inverted by "nand" gate MC44E. The false output of MC44E sets the interrupt inhibit flip-flop MC46C/D. The flip-flop is cleared at time T0, TS of the next machine phase by the false output of MC46A. The true output of the interrupt inhibit flip-flop allows the interrupt control flip-flop to be set. The true set-side output of the interrupt control flip-flop MC35B is applied to "and" gate MC95A along with the output of the interrupt enable flip-flop (MC14C, MC16C) providing a true enable service request signal enabling interrupt signals to the computer.

3-25. SUSPEND PHASE 5. Suspend phase 5 is a one-cycle suspension of normal computer operation which is used by the direct memory access (DMA) option. During a phase 5 operation, the DMA option causes data to be transferred between the computer memory and any selected I/O device, bypassing the interrupt system. A phase 5 must be initiated by the DMA card for each word (16 bits) that is to be transferred to or from the computer.

3-26. When an I/O device being addressed by the DMA option is ready to send or to receive data, it causes the DMA card to generate a false \overline{HIS} (hold interrupt system "not") signal at time T7 of the current machine cycle. The false \overline{HIS} signal is applied to the I/O control card (figure 3-3) where it inhibits the true ESR signal. This disables the interrupt system by preventing a true INT signal from being sent to the computer timing generator card.

3-27. At time T0 of the phase 5 machine cycle, a false $\overline{PH5}$ (Phase 5 "not") signal is applied to the I/O control card from the DMA card. This signal is then inverted and applied to encoders MC75 and MC105 where it prevents T-register bits TR0 through TR5 from being encoded into select codes during phase 5. For phase 5 operation, the select code (address) of the respective external device is generated by the DMA card.

3-28. When the last character word in a block of data (which is predetermined in length) has been transferred to or from the computer, a normal interrupt phase 4 is requested by the DMA card through the interrupt system. To initiate the interrupt, the DMA card applies a true FLG 0 (flag 0) signal to the I/O control card at time T5 of the machine cycle following the last phase 5. This causes "nand" gate MC85A (figure 3-3) to apply a true INT signal to the computer timing generator card. The true INT signal then causes the next machine cycle to be an interrupt phase 4. When the interrupt occurs, a service subroutine performs a predetermined operation (i.e., processes the data which has been transferred to the computer memory) and also returns control of the respective external device to the interrupt system.

3-29. INTERRUPT CONTROL SYSTEM.

3-30. The set or clear condition of the interrupt system enable flip-flop (MC14C, MC16C) determines whether the interrupt system is "on" or "off", under program control. If the flip-flop is set, the IEN signals to the interface cards will enable interrupt requests; if the flip-flop is clear, the IEN signals are removed and interrupt requests will not be enabled. Initially, the interrupt system is disabled by the POPIO signal as described in paragraph 3-6.

3-31. INTERRUPT SYSTEM ENABLE. If the interrupt system is to function, the interrupt enable flip-flop must be set by a STF instruction with a select code of 00. When this is programmed, the SCM(0) and SCL(0) signals, together with the IOG signal, are "anded" by MC95B. The output of MC95B forms the address 00 signal which is applied to one input of "nand" gate MC14A. The STF signal from pin 9 is applied to the other input of MC14A. The false output of MC14A sets the interrupt enable flip-flop.

3-32. The enable service request signal goes true since all inputs to MC95A are now true. The STF 00 signal makes the set-side of the interrupt enable flip-flop true and the interrupt control flip-flop is set at T0, TS providing a true set-side output.

3-33. Refer to figures 2-7 and 3-3. The true set-side output of the interrupt enable flip-flop is applied to "and" gate MC26A and through pin 8 to the interface card slot connectors as a true IEN signal. If both input and output logic is contained on one interface card, the IEN signal enters the card at pin 8 and is then transferred to both logic sections of the card. If there are no interrupt requests to the computer, the true PRL(4) signal from the control

flip-flop is gated through MC43B to become PRH(10). This gives the first I/O interface card a priority high signal. Since it is assumed that no interrupt requests are being made, the priority signal is propagated through the entire string of interface cards uninterrupted. The entire interrupt system is now enabled and interrupt requests can be initiated.

3-34. INTERRUPT SYSTEM DISABLE. To disable the interrupt system, the interrupt enable flip-flop must be cleared by a CLF instruction with a select code of 00. When this is programmed the address 00 signal is again generated and used as one input to MC14B. The CLF signal provides the other input to MC14B. The false output of MC14B clears the interrupt enable flip-flop. The set-side output of the flip-flop goes false, removing the IEN signal to all interface-card slot connectors (see figure 2-7). This immediately prevents any interface card (device) from requesting an interrupt.

3-35. SKIP FLAG INSTRUCTIONS.

3-36. Through the use of the SFS and SFC program instructions, the next instruction in the computer program can be skipped depending on the set or clear condition of the interrupt enable flip-flop. When the interrupt enable flip-flop is set and an SFS instruction is programmed with a select code of 00, all inputs to MC15A are true. MC15A then has a false output which is applied to MC15C. This causes MC15C to output a true signal to "and" gate MC24A. The other input to MC24A is true because the select code 00 causes the address 00 signal to be generated. These two true inputs to MC24A cause a true SKF signal to be sent to the computer. The SKF signal causes the program to skip the next instruction since the interrupt enable flip-flop was set.

3-37. Similarly, when the interrupt enable flip-flop is cleared and an SFC instruction is programmed with a select code of 00, all inputs to "nand" gate MC15D are true sending a false input to MC15C and hence a true signal is taken from MC15C and applied to MC24A. The address 00 signal is again true and MC24A outputs a true SKF signal to the computer. The SKF signal again causes the program to skip the next instruction since in this case, the interrupt enable flip-flop was cleared.

3-38. DECODING FUNCTION.

3-39. When an I/O instruction is programmed, the 6-bit select code portion (bits 0 through 5) of the instruction is received by the I/O control card (figure 3-3). The three least significant bits (0-2) are applied to the binary-to-octal decoder MC75. The octal output of MC75 forms the lower octal digit of the select code. The three most significant bits (3-5) are applied to the binary-to-octal decoder MC105. The octal output of MC105 forms the upper octal digit of the select code.

3-40. The output of the decoders are inverted and go through "nand" gates MC74A through F, MC94A/B and

MC104A/B/E and F. The outputs of these gates will now be true for the desired select code. Each of the outputs of the inverting "nand" gates are buffered out of the I/O control card to the interface cards by "and" gates. These gates provide the drive necessary to apply signals of proper amplitude to the interface cards. The 330 ohm resistor between each of the gates and the -2 volt supply minimizes the effect of any transient noise which may exist on the lines to the interface cards and reduces the fall time of the gate output voltage.

3-41. As an example, with a select code of 11 (001 001 binary) applied to the decoders, only TR0 and TR3 are true input signals. In figure 3-3 each select code digit is produced as follows. The outputs of both decoders are true except for the "octal digit 1" of each decoder which is false; after passing through the inverting "nand" gates only the select code most significant digit (SCM) "1" and select code least significant digit (SCL) "1" are true. These signals are then routed to the interface cards via pins 80 and 64, respectively.

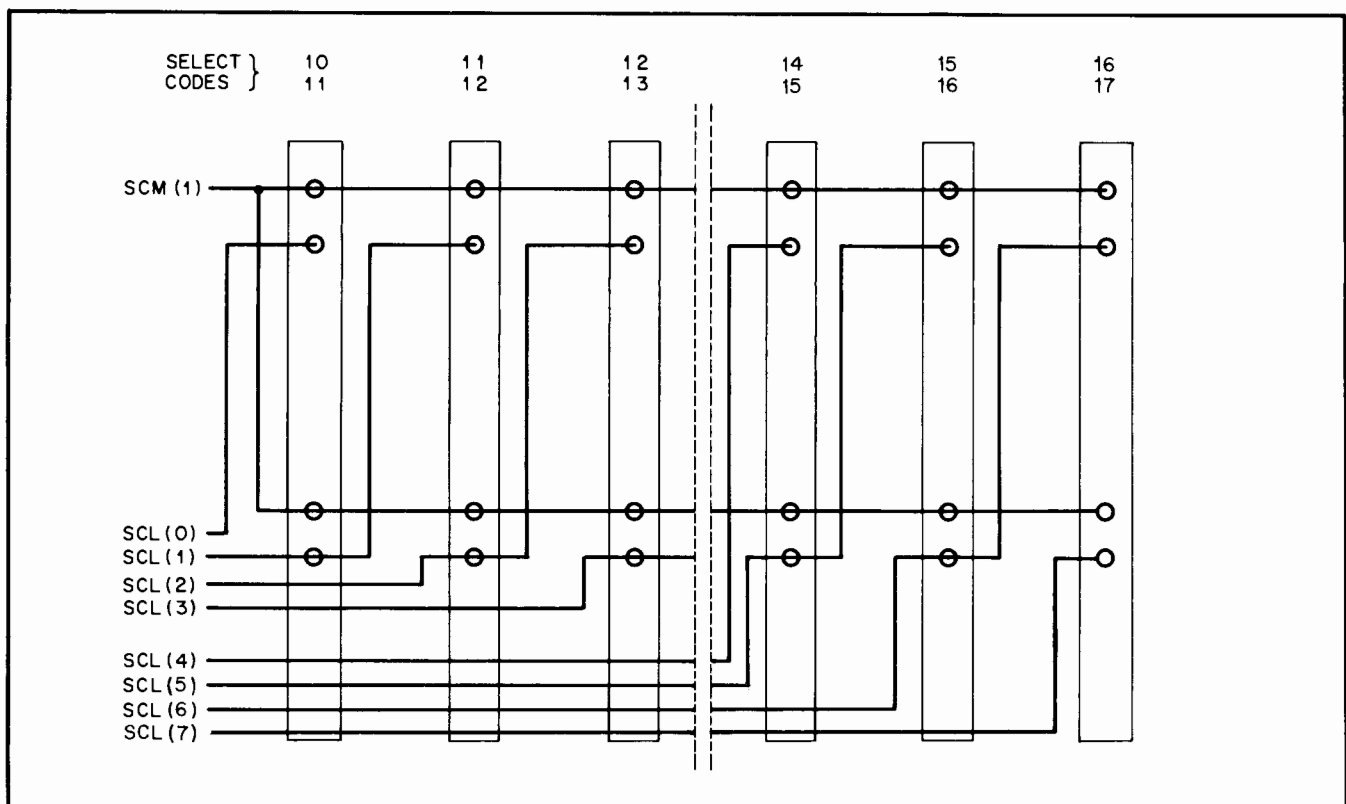
3-42. The SCM and SCL signal combination determines the slot connector containing the interface card to which the instruction portion of the I/O instruction word is directed. Each slot connector, and therefore each interface card, contains two octal select codes as described in section II. Figure 3-1 illustrates the SCM and SCL signal paths to basic computer interface-card slot connectors. Note that the SCM(1) signal is applied to the most-significant-digit input pins on the interface-card slot connectors with select codes of 10 through 16. SCM(1), SCM(2), and SCM(3) are applied through the I/O control card 48-pin connector to extender modules containing interface card slot connectors with select codes of 16 through 37 (see paragraph 2-52). The SCM(0) signal is used on the I/O control card (select codes 00 and 04) and to input from or output data to the switch register (01). The select code 04 is used by the power failure interrupt option. The SCL(0) through SCL(7) signals are applied to the least significant digit input pins on the slot connectors in the computer and in the extender. The slot connectors in the extender are wired in the same manner as those in the basic computer.

3-43. The SCM and SCL signals are applied to the same-numbered pins on all interface card slot connectors as follows:

- a. Pin 14 lower select code, most significant digit.
- b. Pin 16 lower select code, least significant digit.
- c. Pin 37 higher select code, most significant digit.
- d. Pin 34 higher select code, least significant digit.

3-44. ENCODING FUNCTION.

3-45. When an input/output device requests an interrupt of a computer program, the IRQ flip-flop on the interface



2040-4

Figure 3-1. I/O Slot Connector Select Code Wiring

card for the device is set. The set-side output of the IRQ flip-flop applies a true FLG (flag) signal to the I/O control card; the clear-side output of the flip-flop is inverted by an inverting "or" gate to apply a true IRQ signal to the I/O control card. Refer to figure 3-3. These two signals are used to form the interrupt signal and the service request address to be transferred to the computer.

3-46. **INTERRUPT SIGNAL.** An interrupt signal is sent to the computer at time T5 of the current machine phase when a flag signal is received from an interface card and if the enable service request signal is true. (To establish when the enable service request signal is true, refer to figure 2-6.) The interrupt signal causes the computer to enter interrupt phase 4 at the end of the current machine phase, unless the current instruction is a JMP,I, or a JSB,I.

3-47. As shown in figure 3-3, four flag signals (0 through 3) can be received from the interface cards. Three of these flag signals (0 through 2) are used to generate the INT (interrupt) signal. Receipt of one of these flag signals applies a true input to MC64A, MC84A, or MC64D respectively. If the enable service request signal from MC95A is also true a FLG signal (0, 1, or 2) will cause a false input to MC85A. The output of MC85A is then true sending a true interrupt signal to the computer.

3-48. **SERVICE REQUEST ADDRESS.** Refer to figure 3-3. The 6-bit service request address is the select code of the interface card requesting an interrupt, in binary form. It

is sent to the M-register of the computer via the T-bus and specifies the interrupt location for that device in memory. (The interrupt location contains the instruction to be executed when the particular interrupt occurs.) While the interrupt signal is sent to the computer at time T5 of the current machine phase, the service request address is not enabled to the computer until time T7 of interrupt phase 4.

3-49. The service request address is formed by encoding the combination of flag and IRQ signals from the interface card requesting an interrupt. The flag signals form the SCM bit and the IRQ signals form the SCL bit. The IRQ signals are encoded by "nand" gate groups MC53A/B/C/D, MC54A/B/C/D, and MC55A/B/C/D. The outputs of these gate groups are used to set the central interrupt (CI) register flip-flops 0, 1, and 2 respectively. The flag 1, 2, and 3 signals are gated through "nand" gates MC65A, B, and C into CI flip-flops 3, 4, and 5 respectively. At time T7 of interrupt phase 4 the RSM6-9 signal goes true making the RSM6-9 signal on pin 26 false. This signal is inverted by "nand" gate MC94F sending a true clock signal to the CI flip-flops (see next paragraph) setting them to the encoded interrupt address.

3-50. **CENTRAL INTERRUPT REGISTER.**

3-51. The central interrupt register (flip-flops CI0 through CI5 and "nand" gates MC63A/B/C/D, MC64B/C) stores the service request address. This information, or address, is always available during a phase 4 I/O operation

and is strobed into flip-flops CI0 through CI5 at T7 of phase 4. To utilize this address, the computer programmer must execute an I/O load or merge instruction containing a select code of 04. These instructions would be LIA/B and MIA/B used with select code 04. The power fail interrupt select code, 04, is not required during a load instruction and can be used to enable the central interrupt register. On the I/O control card, at T7 phase 4, the RSM6-9 signal drops causing the output of "nand" gate MC94F to be true. This enables the central interrupt register flip-flops allowing the device address to be stored in CI0 through CI5. In order to apply the address to the computer central processor, the IOG signal and the select code 04 are used as inputs for "and" gate MC95C. The output of MC95C is applied to MC85D. When an I/O input instruction is used such as LIA, LIB, MIA, or MIB and the select code 04, then the IOI (input/output input) signal is true. The output of MC85D is then false causing the output of MC85C to be true. The true output of MC85C enables the central interrupt register output gates MC63A/B/C/D and MC64B/C. This applies the contents of the register flip-flops to the IOB lines of the computer central processor. Access to the central interrupt register through programmed instruction will provide the address of the last I/O device that interrupted.

3-52. REPLACEABLE PARTS.

3-53. Refer to table 3-3 for a list of replaceable parts in the alphanumeric order of their reference designations, with a description and HP part number for each part. Refer to table 3-4 for a list of abbreviations used in the DESCRIPTION column. Refer to table 3-5 for a list of codes used in the MFR CODE column.

3-54. To order a replacement part, address the order or inquiry to the local Hewlett-Packard Sales and Service Office. See the list at the back of this manual for addresses.

3-55. Specify the following information for each part when ordering:

- a. Hewlett-Packard part number.
- b. Circuit reference designation.
- c. Description.

3-56. To order a part not listed in table 3-3, give a complete description of the part and include its function and location.

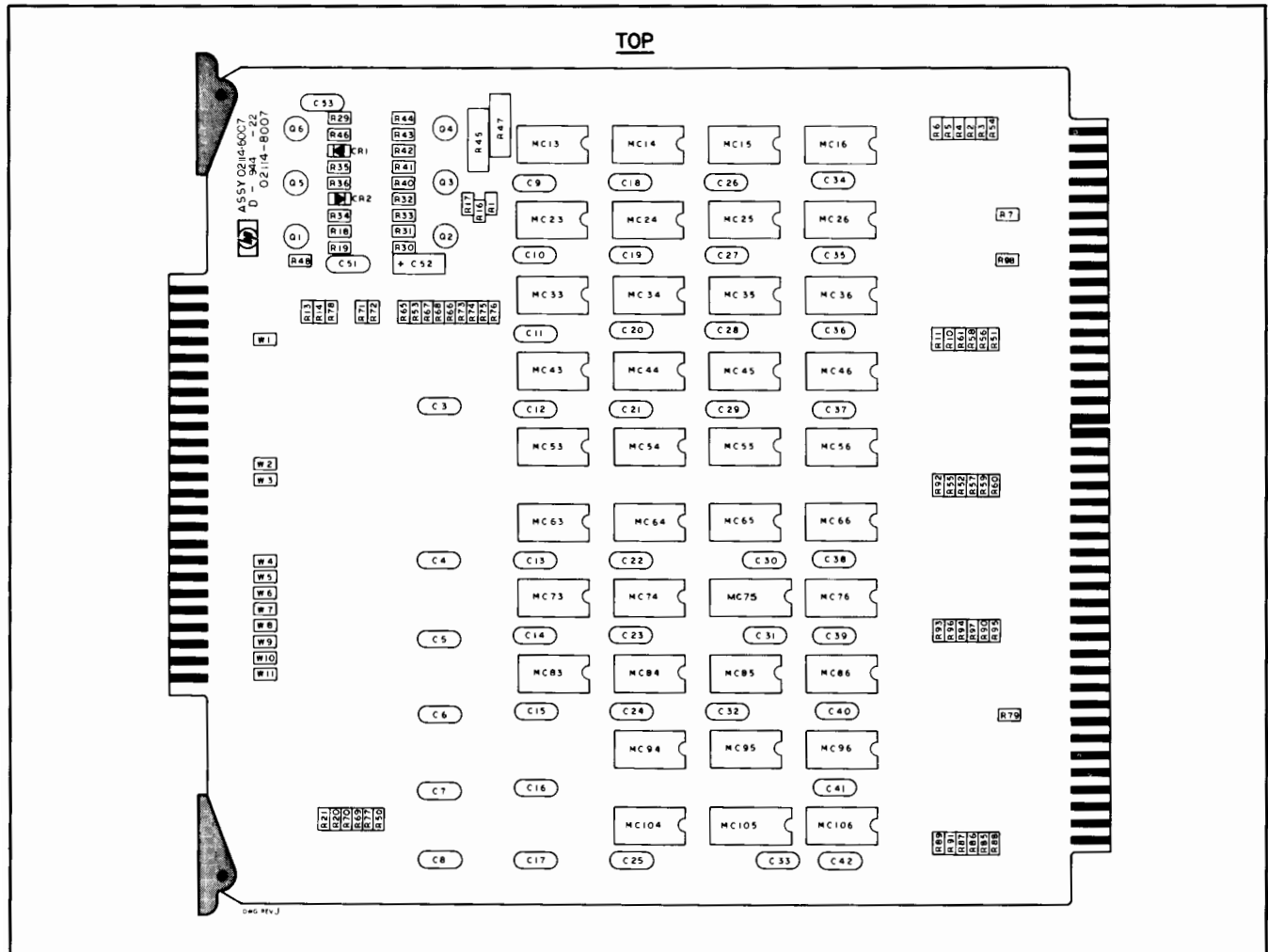


Figure 3-2. Part Location Diagram

Table 3-3. Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C3 thru C42,51,53	0160-2055	Capacitor, Fxd, Cer, 0.01 uf, +80-20%, 100 VDCW	91418	TA
C52	0180-0100	Capacitor, Fxd, Elect. Ta, 4.7uf, 10%, 35 VDCW	56289	150D475X9035B2
CR1	1902-3043	Diode, Breakdown, 3.32V, 2%, 400 mw	28480	1902-3043
CR2	1910-0022	Diode, Germanium, 5 WIV	28480	1910-0022
MC13,23,33,53,54,55,63,64 65,84	1820-0327	Integrated Circuit, TTL	28480	1820-0327
MC14,15,45,46,85	1820-0127	Integrated Circuit, TTL	28480	1820-0127
MC16	1820-0129	Integrated Circuit, TTL	28480	1820-0129
MC24,25,26,56,66,76,86,96, 106	1820-0956	Integrated Circuit, CTL	28480	1820-0956
MC34,35	1820-0077	Integrated Circuit, TTL	28480	1820-0077
MC36,43,95	1820-0372	Integrated Circuit, TTL	28480	1820-0372
MC44,74,94,104	1820-0132	Integrated Circuit, TTL	28480	1820-0132
MC73,83	1820-0301	Integrated Circuit, TTL	28480	1820-0301
MC75,105	1820-0111	Integrated Circuit, TTL	28480	1820-0111
Q1 thru Q6	1854-0215	Transistor, Silicon, NPN	28480	1854-0215
R1,10,11,13,14,17,30,31, 40,41,44,50,65,66,67,68,69 70,71,72,73,74,75,76,77	0683-4715	Resistor, Fxd, Comp, 470 ohm, 5%, 1/4 w	01121	EB 4715
R2,3,4,5,85,86,87,88,89, 90,91,92,93,94,95,96	0683-3315	Resistor Fxd, Comp, 330 ohm, 5%, 1/4 w	01121	CB 3315
R6,18,20,21,29,32,36,51,52, 53,54,55,56,57,58,59,60,61, 78,79,97,98	0683-1025	Resistor, Fxd, Comp, 1000 ohm, 5%, 1/4 w	01121	CB 1025
R7,19,34,42,43	0683-1015	Resistor Fxd Comp, 100 ohm, 5%, 1/4 w	01121	CB 1015
R16,46	0683-3915	Resistor, Fxd, Comp, 390 ohm, 5%, 1/4 w	01121	CB 3915
R33	0683-1005	Resistor, Fxd, Comp, 10 ohm, 5%, 1/4 w	01121	CB 1005
R35	0683-1525	Resistor Fxd, Comp, 1500 ohm, 5%, 1/4 w	01121	CB 01121
R45	0757-0198	Resistor Fxd, Met Flm, 100 ohm, 1%, 1/2 w	28480	0757-0198
R47	0698-3394	Resistor, Fxd, Met Flm, 31.6 ohm, 1% 1/2 w	28480	0698-3394
R48	0683-1825	Resistor, Fxd Comp, 1800 ohm, 5%, 1/4 w	01121	CB 1825
W1 thru W11	8159-0005	Jumper Wire	28480	8159-0005

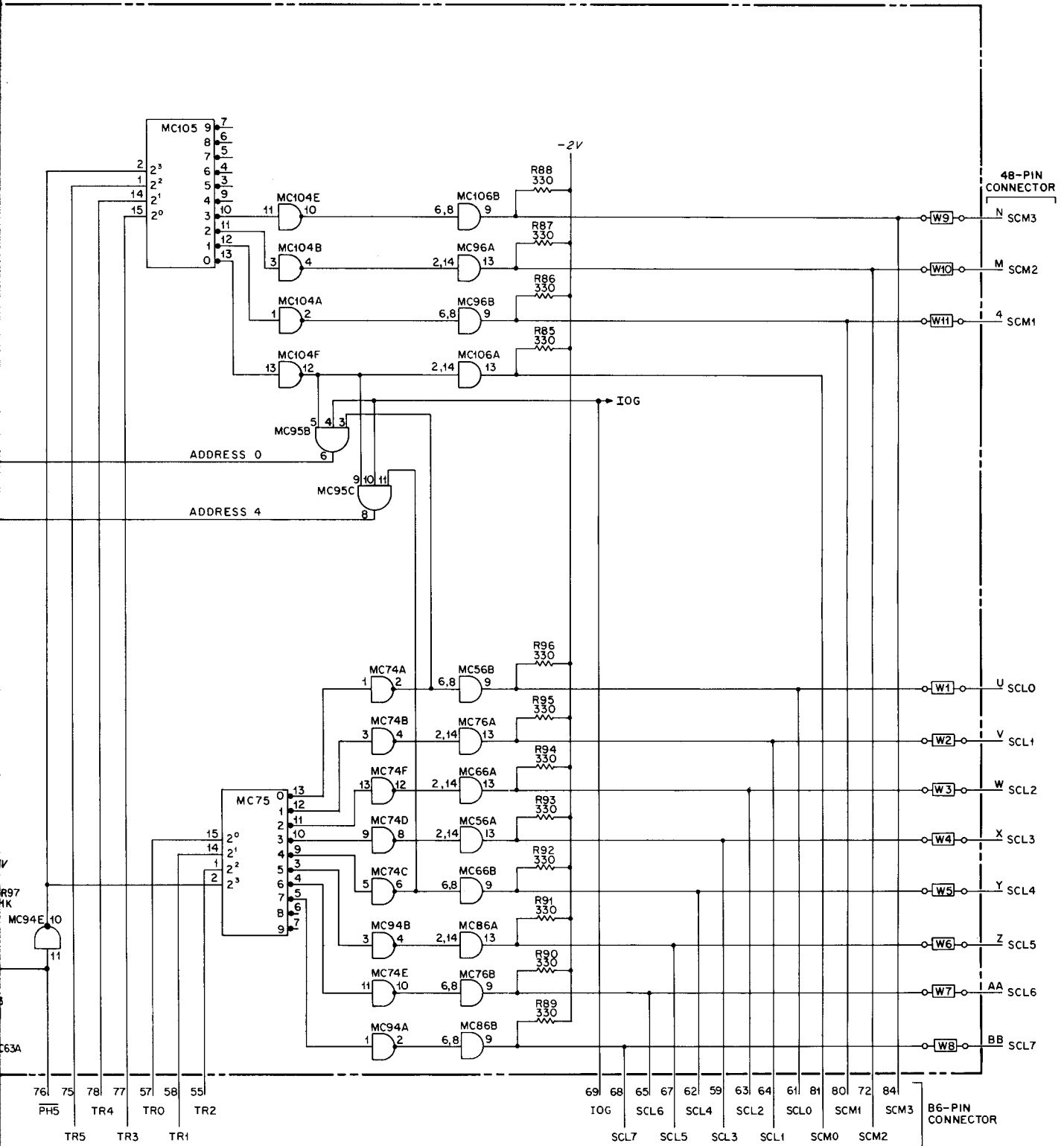
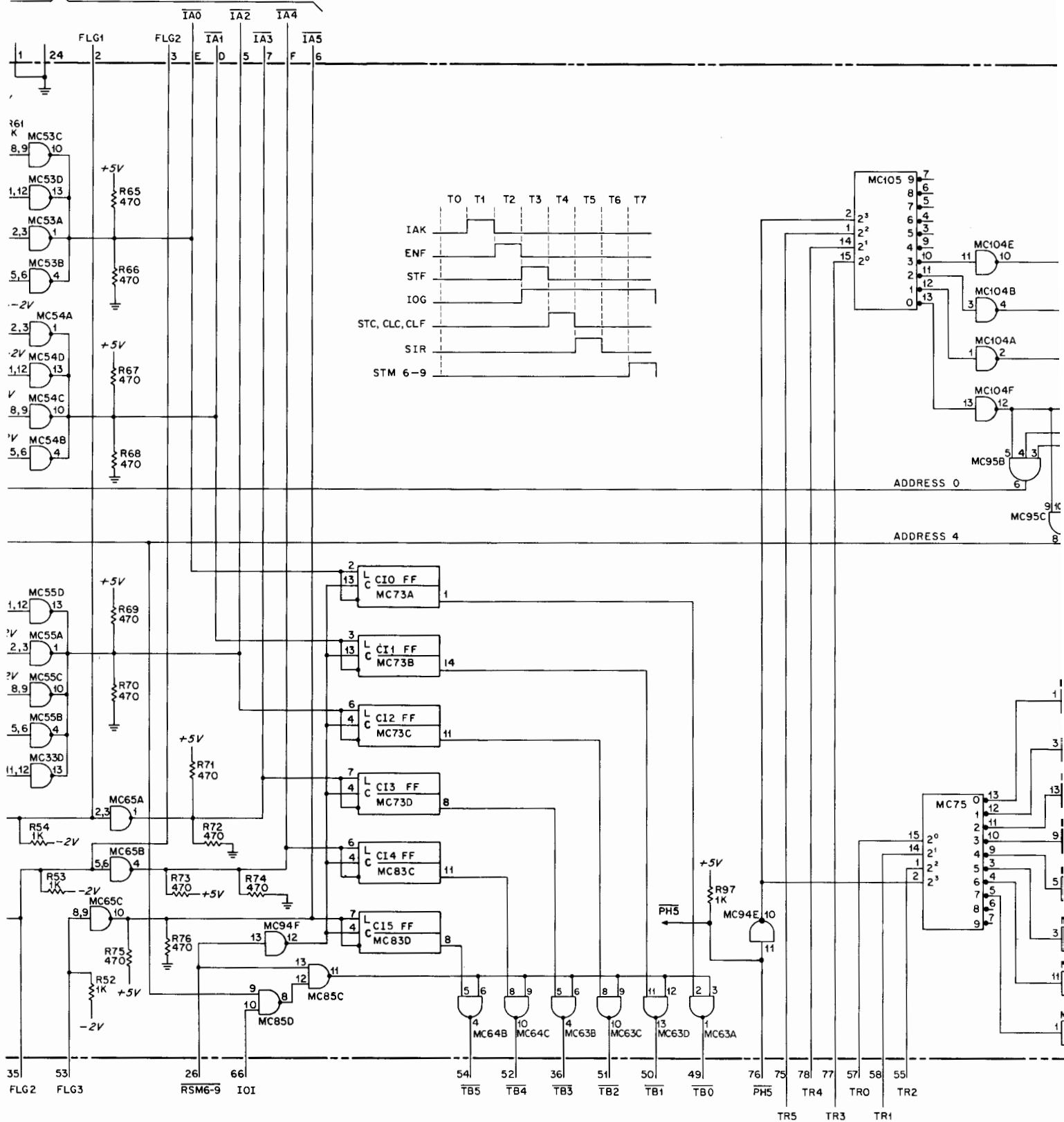


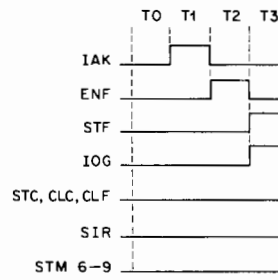
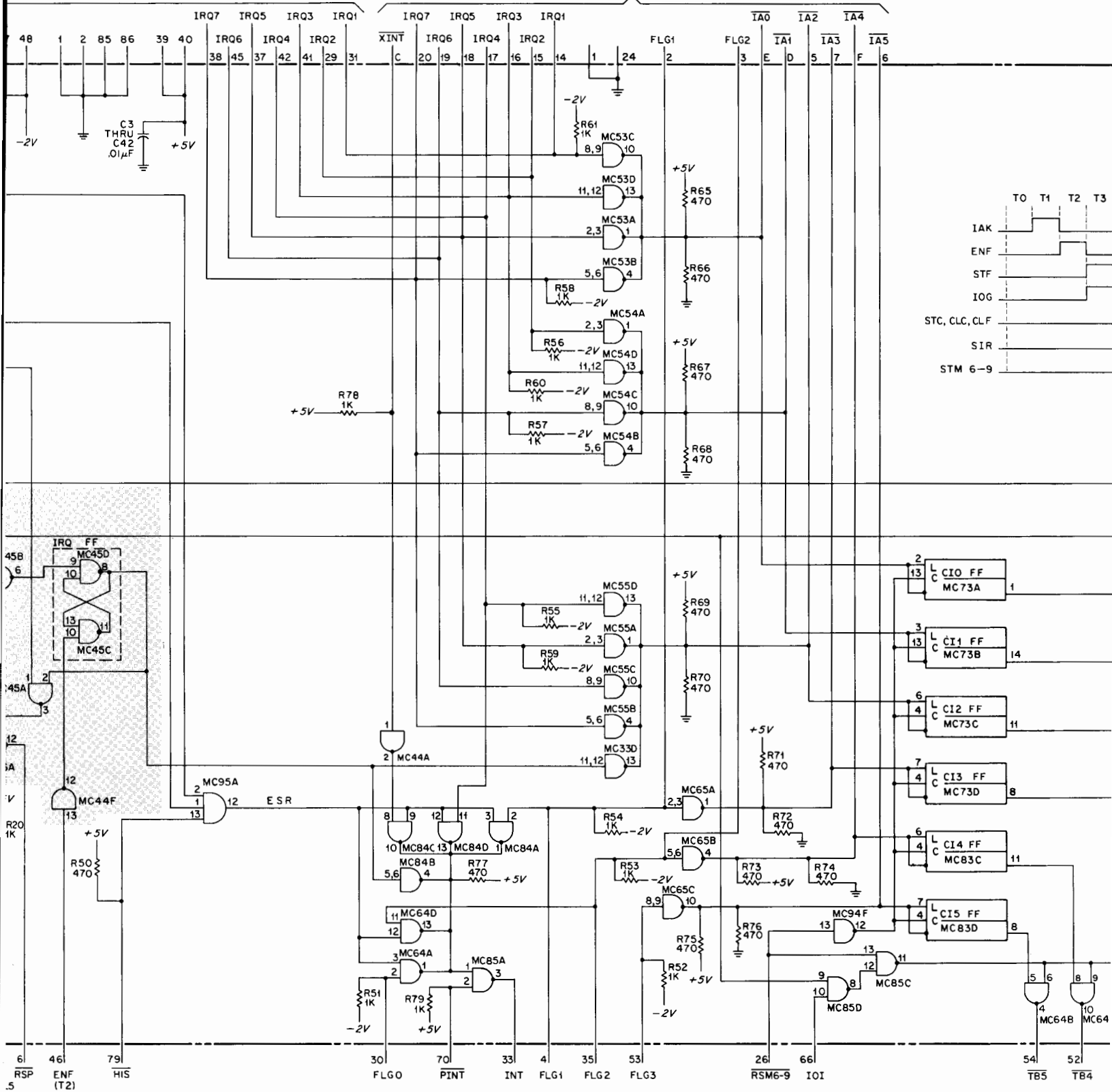
Figure 3-3. I/O Control Card Circuit

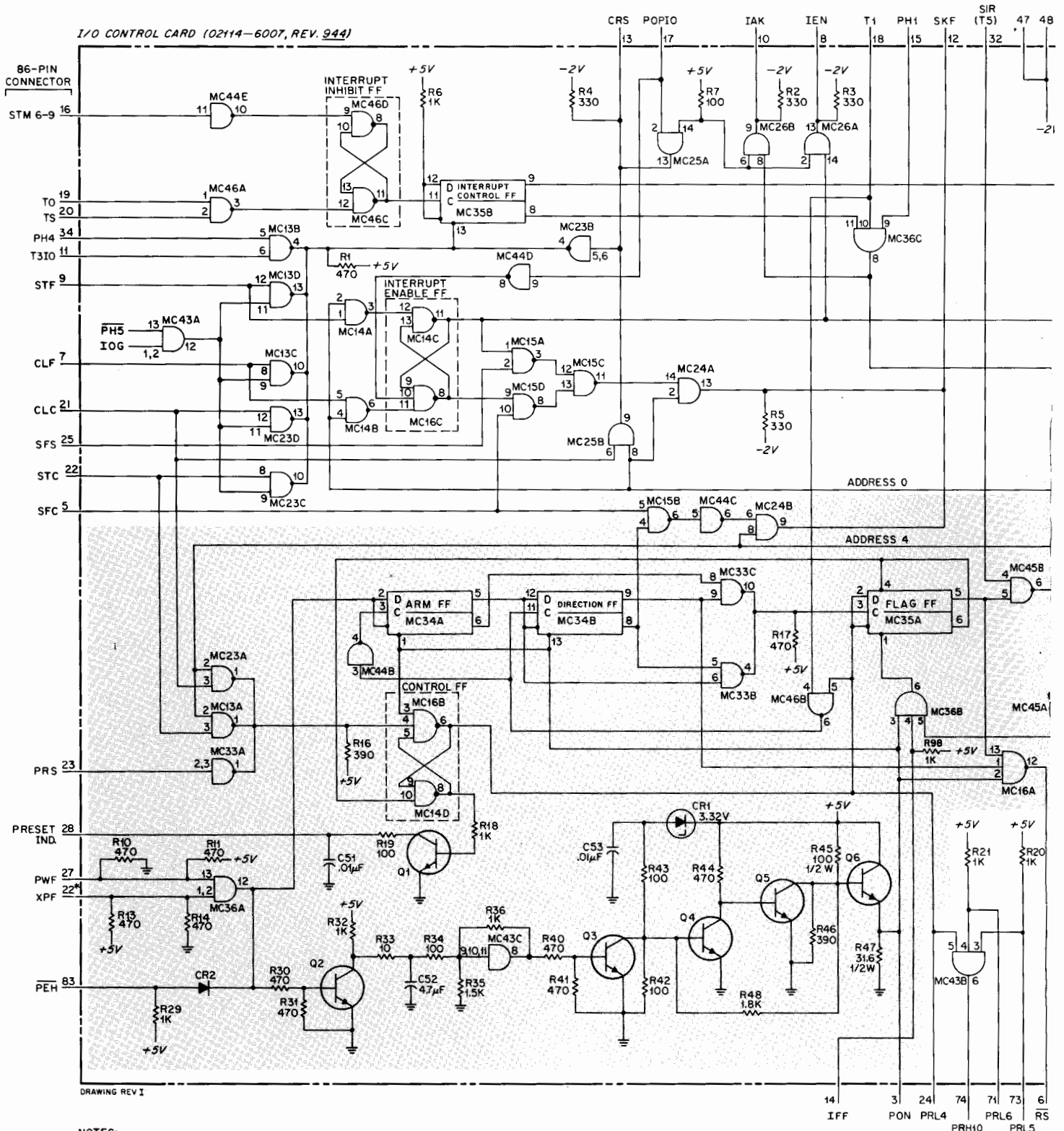
- PIN CONNECTOR



ECTOR

48-PIN CONNECTOR





NOTES:

- 1. SHADED AREA INDICATES POWER FAIL CIRCUITRY.
- * INDICATES 48 PIN CONNECTOR.

Table 3-4. Reference Designations and Abbreviations



REFERENCE DESIGNATIONS		
A = assembly	J = receptacle connector	TB = terminal board
B = motor	K = relay	TP = test point
BT = battery	L = inductor	U = integrated circuit
C = capacitor	M = meter	V = vacuum tube, neon bulb, photocell, etc.
CP = coupler	MC = microcircuit	VR = voltage regulator
CR = diode	P = plug connector	W = cable, jumper
DL = delay line	Q = transistor	X = socket
DS = device signaling (lamp)	R = resistor	Y = crystal
E = misc hardware	RT = thermistor	Z = tuned cavity, network
F = fuse	S = switch	
FL = filter	T = transformer	
ABBREVIATIONS		
A = amperes	IMPG = impregnated	P/O = part of
AC = alternating current	IN. = inch, inches	POLY = polystyrene
AFC = automatic frequency control	INCD = incandescent	PORC = porcelain
ALUM = aluminum	INCL = include(s)	POS = position(s)
AL-ELECT = aluminum electrolytic	INS = insulation(ed)	POT = potentiometer
ASSY = assembly	INT = internal	PP = peak-to-peak
BFO = beat frequency oscillator	I/O = input/output	PT = point
BE CU = beryllium copper	K = kilo = 1000	PWV = peak working voltage
BH = binder head	LH = left hand	R = resistor
BP = bandpass	LIN = linear taper	RECT = rectifier
BRS = brass	LK WASH = lock washer	RF = radio frequency
BWO = backward wave oscillator	LOG = logarithmic taper	RH = round head or right hand
C = capacitor	LPF = low pass filter	RMO = rack mount only
CCW = counterclockwise	M = milli = 10 ⁻³	RMS = root-mean square
CER = ceramic	MEG = mega = 10 ⁶	RWV = reverse working voltage
CMO = cabinet mount only	MET FLM = metal film	S-B = slow-blow
COEF = coefficient	MET OX = metal oxide	SCR = screw
COM = common	MFR = manufacturer	SE = selenium
COMP = composition	MHz = megahertz	SECT = section(s)
COMPL = complete	MINAT = miniature	SEMICON = semiconductor
CONN = connector	MOM = momentary	SI = silicon
CP = cadmium plate	MTG = mounting	SIL = silver
CRT = cathode-ray tube	MY = Mylar	SL = slide
CTL = capacitor-transistor logic	N = nano (10 ⁻⁹)	SPDT = single-pole, double-throw
CW = clockwise	N/C = normally closed	SPG = spring
DC = direct current	NE = neon	SPL = special
DEPC = deposited carbon	NI PL = nickel plate	SPST = single-pole, single-throw
DPDT = double-pole, double-throw	NO. = number	SR = split ring
DPST = double-pole, single-throw	N/O = normally open	SST = stainless steel
DR = drive	NPN = negative-positive-negative	STL = steel
ELECT = electrolytic	NPO = negative positive zero (zero temperature coefficient)	TA = tantalum
ENCAP = encapsulated	NRFR = not recommended for field replacement	TD = time delay
EXT = external	NSR = not separately replaceable	TGL = toggle
F = farads	OBD = order by description	THD = thread
FH = flat head	OD = outer diameter	TI = titanium
FIL H = fillister head	OH = oval head	TOL = tolerance
FXD = fixed	OX = oxide	TRIM = trimmer
G = giga (10 ⁹)	P = peak	TTL = transistor-transistor logic
GE = germanium	PC = printed circuit	TWT = traveling wave tube
GL = glass	PF = picofarads = 10 ⁻¹² farads	U (μ) = micro = 10 ⁻⁶
GND/GRD = ground(ed)	PH = Phillips head	VAR = variable
H = henries	PH BRZ = phosphor bronze	VDCV = direct current working volts
HDW = hardware	PHL = Phillips	W/ = with
HEX = hexagonal	PIV = peak inverse voltage	W = watts
HG = mercury	PNP = positive-negative-positive	WIV = working inverse voltage
HR = hour(s)		WW = wirewound
HZ = hertz		W/O = without
ID = inner diameter		
IF = intermediate frequency		

Table 3-5. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 (Name to Code) and H4-2 (Code to Name) and their latest supplements. The date of revision and the date of the supplements used appear at the bottom of each page. Alphabetical codes have been arbitrarily assigned to suppliers not appearing in the H4 Handbooks.

Code No.	Manufacturer	Address	Code No.	Manufacturer	Address	Code No.	Manufacturer	Address
00000	U. S. A. Common	Any supplier of U. S.	05245	Components Corp.	Chicago, Ill.	09145	Tech. Ind. Inc. Atohm Elect.	Burbank, Calif.
00136	McCoy Electronics	Mount Holly Springs, Pa.	05277	Westinghouse Electric Corp.		09250	Electro Assemblies, Inc.	Chicago, Ill.
00213	Sage Electronics Corp.	Rochester, N. Y.		Semi-Conductor Dept.	Youngwood, Pa.	09353	C & K Components Inc.	Newton, Mass.
00287	Cenco Inc.	Danielson, Conn.	05347	Ultronix, Inc.	San Mateo, Calif.	09569	Mallory Battery Co. of	
00334	Humidial	Colton, Calif.	05397	Union Carbide Corp., Elect. Div.			Canada, Ltd.	Toronto, Ontario, Canada
00348	Microtron Co., Inc.	Valley Stream, N. Y.			New York, N. Y.	09922	Burndy Corp.	Norwalk, Conn.
00373	Garlock Inc.	Cherry Hill, N. J.	05574	Viking Ind. Inc.	Canoga Park, Calif.	10214	General Transistor Western Corp.	
00656	Aerovox Corp.	New Bedford, Mass.	05593	Icore Electro-Plastics Inc.	Sunnyvale, Calif.			Los Angeles, Calif.
00779	Amp. Inc.	Harrisburg, Pa.	05616	Cosmo Plastic		10411	Ti-Tal, Inc.	Berkeley, Calif.
00781	Aircraft Radio Corp.	Boonton, N. J.		(c/o Electrical Spec. Co.)	Cleveland, Ohio	10646	Carborundum Co.	Niagara Falls, N. Y.
00815	Northern Engineering Laboratories, Inc.	Burlington, Wis.	05624	Barber Colman Co.	Rockford, Ill.	11236	CTS of Berne, Inc.	Berne, Ind.
			05728	Tiffen Optical Co.		11237	Chicago Telephone of California, Inc.	
00853	Sangamo Electric Co., Pickens Div.	Pickens, S. C.			Roslyn Heights, Long Island, N. Y.			So. Pasadena, Calif.
00866	Goe Engineering Co.	City of Industry, Cal.	05729	Metro-Tel Corp.	Westbury, N. Y.	11242	Bay State Electronics Corp.	Waltham, Mass.
00891	Carl E. Holmes Corp.	Los Angeles, Calif.	05783	Stewart Engineering Co.	Santa Cruz, Calif.	11312	Teledyne Inc., Microwave Div.	Palo Alto, Calif.
00929	Microfab Inc.	Livingston, N. J.	05820	Wakfield Engineering Inc.	Wakfield, Mass.	11314	National Seal	Downey, Calif.
01002	General Electric Co., Capacitor Dept.		06004	Bassick Co., Div. of Stewart Warner Corp.		11453	Precision Connector Corp.	Jamaica, N. Y.
		Hudson Falls, N. Y.			Bridgeport, Conn.	11534	Duncan Electronics Inc.	Costa Mesa, Calif.
01009	Alden Products Co.	Brockton, Mass.	06090	Raychem Corp.	Redwood City, Calif.	11711	General Instrument Corp., Semiconductor	
01121	Allen Bradley Co.	Milwaukee, Wis.	06175	Bausch and Lomb Optical Co.	Rochester, N. Y.		Div., Products Group	Newark, N. J.
01255	Litton Industries, Inc.	Beverly Hills, Calif.	06402	E. T. A. Products Co. of America	Chicago, Ill.	11717	Imperial Electronic, Inc.	Buena Park, Calif.
01281	TRW Semiconductors, Inc.	Lawndale, Calif.	06540	Amatom Electronic Hardware Co., Inc.		11870	Metabs, Inc.	Palo Alto, Calif.
01295	Texas Instruments, Inc., Transistor Products Div.	Dallas, Texas	06555	Beede Electrical Instrument Co., Inc.	New Rochelle, N. Y.	12040	National Semiconductor	Danbury, Conn.
01349	The Alliance Mfg. Co.	Alliance, Ohio	06666	General Devices Co., Inc.	Indianapolis, Ind.	12136	Philadelphia Handle Co.	Camden, N. J.
01589	Pacific Relays, Inc.	Van Nuys, Calif.	06751	Components Inc., Ariz. Div.	Phoenix, Ariz.	12361	Grove Mfg. Co., Inc.	Shady Grove, Pa.
01670	Gudebrod Bros. Silk Co.	New York, N. Y.	06812	Torrington Mfg. Co., West Div.		12574	Gulton Ind. Inc. Data System Div.	Albuquerque, N. M.
01930	Amerock Corp.	Rockford, Ill.			Van Nuys, Calif.	12697	Clarostat Mfg. Co.	Dover, N. H.
01961	Pulse Engineering Co.	Santa Clara, Calif.	06980	Varian Assoc. Eimac Div.	San Carlos, Calif.	12728	Eimar Filter Corp.	W. Haven, Conn.
02114	Ferroxcube Corp. of America	Saugerties, N. Y.	07088	Kelvin Electric Co.	Van Nuys, Calif.	12859	Nippon Electric Co., Ltd.	Tokyo, Japan
02116	Wheelock Signals, Inc.	Long Branch, N. J.	07126	Digitran Co.	Pasadena, Calif.	12881	Metex Electronics Corp.	Clark, N. J.
02286	Cole Rubber and Plastics Inc.	Sunnyvale, Calif.	07137	Transistor Electronics Corp.	Minneapolis, Minn.	12930	Delta Semiconductor Inc.	Newport Beach, Calif.
02660	Amphenol-Borg Electronics Corp.	Broadview, Ill.	07138	Westinghouse Electric Corp.		12954	Dickson Electronics Corp.	Scottsdale, Arizona
02735	Radio Corp. of America, Semiconductor and Materials Div.	Somerville, N. J.		Electronic Tube Div.	Elmira, N. Y.	13103	Thermolloy	Dallas, Texas
			07149	Filmohm Corp.	New York, N. Y.	13396	Telefunken (GmbH)	Hanover, Germany
02771	Vocafine Co. of America, Inc.		07233	Cinch-Graphix Co.	City of Industry, Calif.	13835	Midland-Wright Div. of Pacific Industries, Inc.	Kansas City, Kansas
		Old Saybrook, Conn.	07256	Silicon Transistor Corp.	Carle Place, N. Y.	14099	Sem-Tech	Newbury Park, Calif.
02777	Hopkins Engineering Co.	San Fernando, Calif.	07261	Avnet Corp.	Culver City, Calif.	14193	Calif. Resistor Corp.	Santa Monica, Calif.
02875	Hudson Tool & Die Co.	Newark, N. J.	07263	Fairchild Camera & Inst. Corp.		14298	American Components, Inc.	Conshohocken, Pa.
03508	G. E. Semiconductor Prod. Dept.	Syracuse, N. Y.		Semiconductor Div.	Mountain View, Calif.	14433	ITT Semiconductor, A Div. of Int. Telephone & Telegraph Corp.	West Palm Beach, Fla.
03705	Apex Machine & Tool Co.	Dayton, Ohio	07322	Minnesota Rubber Co.	Minneapolis, Minn.	14493	Hewlett-Packard Company	Loveland, Colo.
03797	Eldema Corp.	Compton, Calif.	07387	Bitcher Corp., The	Monterey Park, Calif.	14655	Cornell Dublier Electric Corp.	Newark, N. J.
03818	Parker Seal Co.	Los Angeles, Calif.	07397	Sylvania Elect. Prod. Inc., Mt. View Operations	Mountain View, Calif.	14674	Conning Glass Works	Corning, N. Y.
03877	Transitron Electric Corp.	Wakfield, Mass.			Cranford, N. J.	14752	Electro Cube Inc.	San Gabriel, Calif.
03888	Pyrofilm Resistor Co., Inc.	Cedar Knolls, N. J.	07700	Technical Wire Products Inc.	Chicago, Ill.	14960	Williams Mfg. Co.	San Jose, Calif.
03954	Singer Co., Diehl Div.		07829	Bodine Elect. Co.	Chicago, Ill.	15203	Webster Electronics Co.	New York, N. Y.
	Finderne Plant	Sumerville, N. J.	07910	Continental Device Corp.	Hawthorne, Calif.	15287	Scionics Corp.	Northridge, Calif.
04009	Arrow, Hart and Hegeman Elect. Co.		07933	Raytheon Mfg. Co., Semiconductor Div.	Mountain View, Calif.	15291	Adjustable Bushing Co.	N. Hollywood, Calif.
		Hartford, Conn.	07980	Hewlett-Packard Co., Boonton Radio Div.	Rockaway, N. J.	15558	Micron Electronics	Garden City, Long Island, N. Y.
04013	Taurus Corp.	Lambertville, N. J.			Los Angeles, Calif.	15566	Amprobe Inst. Corp.	Lynbrook, N. Y.
04062	Aico Electronic Inc.	Great Neck, N. Y.	08145	U. S. Engineering Co.	Pomona, Calif.	15631	Cabletronics	Costa Mesa, Calif.
04222	Hi-Q Division of Aerovox	Myrtle Beach, S. C.	08289	Blinn, Delbert Co.		15772	Twentieth Century Coil Spring Co.	Santa Clara, Calif.
04354	Precision Paper Tube Co.	Wheeling, Ill.	08358	Burgess Battery Co.				Framingham, Mass.
04404	Dymec Division of Hewlett-Packard Co.	Palo Alto, Calif.			Niagara Falls, Ontario, Canada	15801	Fenwal Elect. Inc.	Mt. View, Calif.
04651	Sylvania Electric Products, Microwave Device Div.	Mountain View, Calif.	08524	Deutsch Fastener Corp.	Los Angeles, Calif.	16037	Spruce Pine Mica Co.	Spruce Pine, N. C.
04673	Dakota Engr. Inc.	Culver City, Calif.	08664	Bristol Co., The	Waterbury, Conn.	16179	Omni-Spectra Inc.	Farmington, Mich.
04713	Motorola, Inc., Semiconductor Prod. Div.	Phoenix, Arizona	08717	Stoan Company	Sun Valley, Calif.	16352	Computer Diode Corp.	Lodi, N. J.
			08718	ITT Cannon Electric Inc., Phoenix Div.	Phoenix, Arizona	16585	Boots Aircraft Nut Corp.	Pasadena, Calif.
04732	Filtron Co., Inc. Western Div.	Culver City, Calif.	08727	National Radio Lab. Inc.	Paramus, N. J.	16688	Ideal Prec. Meter Co., Inc.	
		Northlake, Ill.	08792	CBS Electronics Semiconductor Operations, Div. of C. B. S. Inc.			De Jur Meter Div.	Brooklyn, N. Y.
04773	Automatic Electric Co.	Northlake, Ill.			Lowell, Mass.	16758	Delco Radio Div. of G. M. Corp.	Kokoma, Ind.
04796	Sequoia Wire Co.	Redwood City, Calif.	08806	General Electric Co. Miniat. Lamp Dept.		17109	Thermometrics Inc.	Canoga Park, Calif.
04811	Precision Coil Spring Co.	El Monte, Calif.			Cleveland, Ohio	17474	Tranex Company	Mountain View, Calif.
04870	P. M. Motor Company	Westchester, Ill.	08984	Mel-Rain	Indianapolis, Ind.	17554	Components Inc.	Biddeford, Ma.
04919	Component Mfg. Service Co.		09026	Babcock Relays Div.	Costa Mesa, Calif.	17675	HamiIn Metal Products Corp.	Akron, Ohio
		W. Bridgewater, Mass.	09134	Texas Capacitor Co.	Houston, Texas	17745	Amstrohm Prec. Inc.	No. Hollywood, Calif.
05006	Twentieth Century Plastics, Inc.	Los Angeles, Calif.						

Table 3-5. Code List of Manufacturers (Continued)

Code No.	Manufacturer	Address	Code No.	Manufacturer	Address	Code No.	Manufacturer	Address
17870	McGraw-Edison Co.	Manchester, N. H.	62119	Universal Electric Co.	Owosso, Mich.	73899	JFD Electronics Corp.	Brooklyn, N. Y.
18042	Power Design Pacific Inc.	Palo Alto, Calif.	63743	Ward-Leonard Electric Co.	ML Vernon, N. Y.	73905	Jennings Radio Mfg. Corp.	San Jose, Calif.
18083	Clevite Corp., Semiconductor Div.	Palo Alto, Calif.	64959	Western Electric Co., Inc.	New York, N. Y.	73957	Groov-Pin Corp.	Ridgefield, N. J.
18324	Signetics Corp.	Sunnyvale, Calif.	65092	Weston Inst. Inc. Weston-Newark	Newark, N. J.	74276	Signalite Inc.	Neptune, N. J.
18476	Ty-Car Mfg. Co., Inc.	Holliston, Mass.	66295	Wittek Mfg. Co.	Chicago, Ill.	74455	J. H. Winns, and Sons	Winchester, Mass.
18486	TRW Elect. Comp. Div.	Des Plaines, Ill.	66346	Minnesota Mining & Mfg. Co. Revere	Mincon Div. St. Paul, Minn.	74861	Industrial Condenser Corp.	Chicago, Ill.
18583	Curtis Instrument, Inc.	Mt. Kisco, N. Y.	70276	Allen Mfg. Co.	Hartford, Conn.	74868	R. F. Products Division of Amphenol-Borg	Danbury, Conn.
18612	Vishay Instruments Inc.	Malvern, Pa.	70309	Allied Control	New York, N. Y.	74970	E. F. Johnson Co.	Waseca, Minn.
18873	E. I. DuPont and Co., Inc.	Wilmington, Del.	70318	Allmetal Screw Product Co., Inc.	Garden City, N. Y.	75042	International Resistance Co.	Philadelphia, Pa.
18911	Durant Mfg. Co.	Milwaukee, Wis.	70417	Amplex, Div. of Chrysler Corp.	Detroit, Mich.	75263	Keystone Carbon Co., Inc.	St. Marys, Pa.
19315	The Bendix Corp., Navigation & Control Div.	Teterboro, N. J.	70485	Atlantic India Rubber Works, Inc.	Chicago, Ill.	75378	CTS Knights Inc.	Sandwich, Ill.
19500	Thomas A. Edison Industries, Div. of McGraw-Edison Co.	West Orange, N. J.	70563	Amperite Co., Inc.	Union City, N. J.	75382	Kulka Electric Corporation	Mt. Vernon, N. Y.
19589	Concoa	Baldwin Park, Calif.	70674	ADC Products Inc.	Minneapolis, Minn.	75818	Lenz Electric Mfg. Co.	Chicago, Ill.
19644	LRC Electronics	Horseheads, N. Y.	70903	Belden Mfg. Co.	Chicago, Ill.	75915	Littlefuse, Inc.	Des Plaines, Ill.
19701	Electra Mfg. Co.	Independence, Kansas	70998	Bird Electronic Corp.	Cleveland, Ohio	76005	Lord Mfg. Co.	Erie, Pa.
20183	General Altronics Corp.	Philadelphia, Pa.	71002	Birnbach Radio Co.	New York, N. Y.	76210	C. W. Marwedel	San Francisco, Calif.
21226	Executone, Inc.	Long Island City, N. Y.	71034	Bliley Electric Co., Inc.	Erie, Pa.	76433	General Instrument Corp., Micamold Division	Newark, N. J.
21335	Falnir Bearing Co., The	New Britain, Conn.	71041	Boston Gear Works Div. of Murray Co. of Texas	Quincy, Mass.	76487	James Millen Mfg. Co., Inc.	Malden, Mass.
21520	Fansteel Metallurgical Corp.	N. Chicago, Ill.	71218	Bud Radio, Inc.	Willoughby, Ohio	76493	J. W. Miller Co.	Los Angeles, Calif.
23042	Texascan Corp.	Indianapolis, Ind.	71279	Cambridge Thermionics Corp.	Cambridge, Mass.	76530	Cinch-Monadnock, Div. of United Carr	San Leandro, Calif.
23783	British Radio Electronics Ltd.	Washington, D. C.	71286	Camloc Fastener Corp.	Paramus, N. J.	76545	Mueller Electric Co.	Cleveland, Ohio
24455	G. E. Lamp Division	Nela Park, Cleveland, Ohio	71313	Cardwell Condenser Corp.	Lindenhurst L. I., N. Y.	76703	National Union	Newark, N. J.
24655	General Radio Co.	West Concord, Mass.	71400	Bussmann Mfg. Div. of McGraw-Edison Co.	St. Louis, Mo.	76854	Oak Manufacturing Co.	Crystal Lake, Ill.
24681	Memcor Inc., Comp. Div.	Huntington, Ind.	71436	Chicago Condenser Corp.	Chicago, Ill.	77068	The Bendix Corp., Electrodynamic Div.	N. Hollywood, Calif.
24796	Parfeco Inc.	San Juan Capistrano, Calif.	71447	Calif. Spring Co., Inc.	Pico-Rivera, Calif.	77075	Pacific Metals Co.	San Francisco, Calif.
26365	Gries Reproducer Corp.	New Rochelle, N. Y.	71450	CTS Corp.	Elkhart, Ind.	77221	Phanostran Instrument and Electronic Co.	South Pasadena, Calif.
26462	Grobet File Co. of America, Inc.	Carlstadt, N. J.	71468	ITT Cannon Electric Inc.	Los Angeles, Calif.	77252	Philadelphia Steel and Wire Corp.	Philadelphia, Pa.
26851	Compac/Hollister Co.	Hollister, Calif.	71471	Cinema, Div. Aerovox Corp.	Burbank, Calif.	77342	American Machine & Foundry Co. Potter	Princeton, Ind.
26992	Hamilton Watch Co.	Lancaster, Pa.	71482	C. P. Clare & Co.	Chicago, Ill.	77630	TRW Electronic Components Div.	Camden, N. J.
27251	Specialities Mfg. Co., Inc.	Stratford, Conn.	71590	Centralab Div. of Globe Union Inc.	Milwaukee, Wis.	77638	General Instrument Corp., Rectifier Div.	Brooklyn, N. Y.
28480	Hewlett-Packard Co.	Palo Alto, Calif.	71616	Commercial Plastics Co.	Chicago, Ill.	77764	Resistance Products Co.	Harrisburg, Pa.
28520	Heyman Mfg. Co.	Kenilworth, N. J.	71700	Cornish Wire Co., The	New York, N. Y.	77969	Rubbercraft Corp. of Calif.	Torrance, Calif.
30817	Instrument Specialities Co., Inc.	Little Falls, N. J.	71707	Coto Coil Co., Inc.	Providence, R. I.	78189	Shakeproof Division of Illinois Tool Works	Elgin, Ill.
33173	G. E. Receiving Tube Dept.	Owensboro, Ky.	71744	Chicago Miniature Lamp Works	Chicago, Ill.	78277	Sigma	So. Braintree, Mass.
35434	Lectrohm Inc.	Chicago, Ill.	71785	Cinch Mfg. Co., Howard B. Jones Div.	Chicago, Ill.	78283	Signal Indicator Corp.	New York, N. Y.
36196	Stanwyck Coil Products Ltd.	Hawkesbury, Ontario, Canada	71984	Dow Corning Corp.	Midland, Mich.	78290	Struthers-Dunn Inc.	Pittman, N. J.
36287	Cunningham, W. H. & Hill, Ltd.	Toronto Ontario, Canada	72136	Electro Motive Mfg. Co., Inc.	Williamant, Conn.	78424	Speciality Leather Prod. Co.	Newark, N. J.
37942	P. R. Mallory & Co. Inc.	Indianapolis, Ind.	72619	Dialight Corp.	Brooklyn, N. Y.	78452	Thompson-Bremer & Co.	Chicago, Ill.
39543	Mechanical Industries Prod. Co.	Akron, Ohio	72656	Indiana General Corp., Electronics Div.	Keasby, N. J.	78471	Tilley Mfg. Co.	San Francisco, Calif.
40920	Miniature Precision Bearings, Inc.	Keene, N. H.	72699	General Instrument Corp., Cap. Div.	Newark, N. J.	78488	Stackpole Carbon Co.	St. Marys, Pa.
42190	Muter Co.	Chicago, Ill.	72765	Drake Mfg. Co.	Harwood Heights, Ill.	78493	Standard Thomson Corp.	Waltham, Mass.
43990	C. A. Norgren Co.	Englewood, Colo.	72825	Hugh H. Eby Inc.	Philadelphia, Pa.	78553	Tinnerman Products, Inc.	Cleveland, Ohio
44655	Ohmite Mfg. Co.	Skokie, Ill.	72928	Gudeman Co.	Chicago, Ill.	78790	Transformer Engineers	San Gabriel, Calif.
46384	Penn Eng. & Mfg. Corp.	Doylestown, Pa.	72962	Elastic Stop Nut Corp.	Union, N. J.	78947	Uconite Co.	Newtownville, Mass.
47904	Polaroid Corp.	Cambridge, Mass.	72964	Robert M. Hadley Co.	Los Angeles, Calif.	79136	Waldes Kohnoor Inc.	Long Island City, N. Y.
48620	Precision Thermometer & Inst. Co.	Southampton, Pa.	72982	Erie Technological Products, Inc.	Erie, Pa.	79142	Veeder Root, Inc.	Hartford, Conn.
49956	Microwave & Power Tube Div.	Waltham, Mass.	73061	Hansen Mfg. Co., Inc.	Princeton, Ind.	79251	Wenco Mfg. Co.	Chicago, Ill.
52090	Rowan Controller Co.	Westminster, Md.	73076	H. M. Harper Co.	Chicago, Ill.	79727	Continental-Wirt Electronics Corp.	Philadelphia, Pa.
52983	Sanborn Company	Waltham, Mass.	73138	Helipot Div. of Beckman Inst., Inc.	Fullerton, Calif.	79963	Zierick Mfg. Corp.	New Rochelle, N. Y.
54294	Shallcross Mfg. Co.	Selma, N. C.	73293	Hughes Products Division of Hughes Aircraft Co.	Newport Beach, Calif.	80031	Mepro Division of Sessions Clock Co.	Morristown, N. J.
55026	Simpson Electric Co.	Chicago, Ill.	73445	Ampetex Elect. Co.	Hicksville, L. I., N. Y.	80120	Schnitzer Alloy Products Co.	Elizabeth, N. J.
55933	Sonotone Corp.	Elmsford, N. Y.	73506	Bradley Semiconductor Corp.	New Haven, Conn.	80131	Electronic Industries Association. Any brand	Tube meeting EIA Standards-Washington, DC.
55938	Raytheon Co. Commercial Apparatus & Systems Div.	So. Norwalk, Conn.	73559	Carling Electric, Inc.	Hartford, Conn.	80207	Unimax Switch, Div. Maxon Electronics Corp.	Wallingford, Conn.
56137	Spaulding Fibre Co., Inc.	Tonawanda, N. Y.	73586	Circle F Mfg. Co.	Trenton, N. J.	80223	United Transformer Corp.	New York, N. Y.
56289	Sprague Electric Co.	North Adams, Mass.	73682	George K. Garrett Co., Div. MSL Industries Inc.	Philadelphia, Pa.	80248	Oxford Electric Corp.	Chicago, Ill.
59446	Telex Corp.	Tulsa, Okla.	73734	Federal Screw Products Inc.	Chicago, Ill.	80294	Bourns Inc.	Riverside, Calif.
59730	Thomas & Betts Co.	Elizabeth, N. J.	73743	Fischer Special Mfg. Co.	Cincinnati, Ohio	80411	Acro Div. of Robertshaw Controls Co.	Columbus, Ohio
60741	Triplet Electrical Inst. Co.	Bluffton, Ohio	73793	General Industries Co., The	Elyria, Ohio			
61775	Union Switch and Signal, Div. of Westinghouse Air Brake Co.	Pittsburgh, Pa.	73846	Goshen Stamping & Tool Co.	Goshen, Ind.			

Table 3-5. Code List of Manufacturers (Continued)

Table with 3 columns: Code No., Manufacturer, Address. Contains multiple rows of manufacturer data including All Star Products Inc., Avery Label Co., etc. Includes a section for vendors with no number assigned.

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