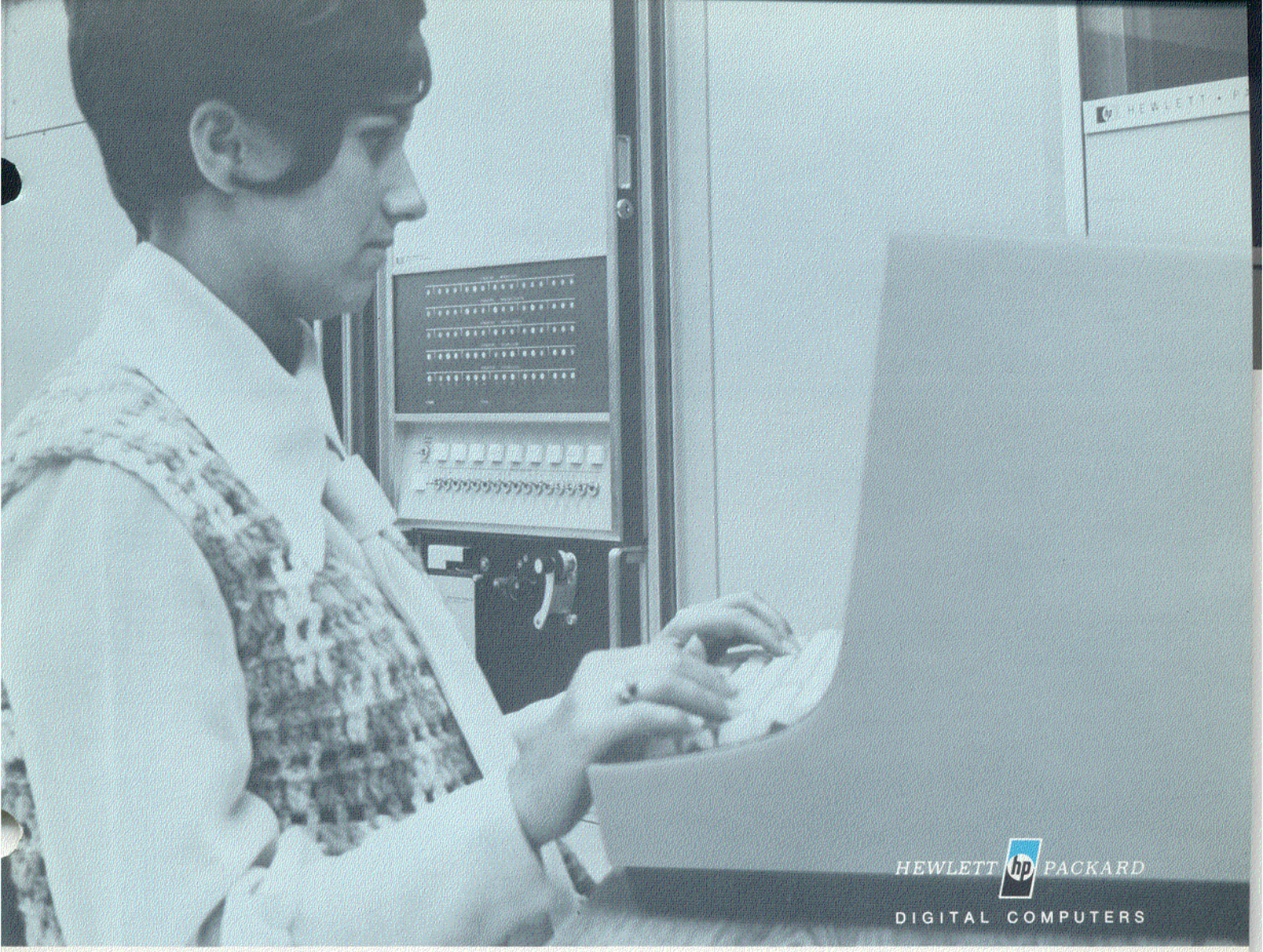


2116C COMPUTER

- **LARGE INTERNAL MEMORY**
  Provides you with a minimum of 8192 words, expandable to 32,768 words *all in mainframe*
- **VERSATILE INPUT/OUTPUT**
  Transfers 16-bit words in parallel over 16 separate channels (optional extenders let you add 16 or 32 more channels)
- **FULL INTERRUPT SYSTEM**
  Permits you to easily establish and change interrupt priority for *all* channels
- **PLUG-IN INTERFACE**
  Simplifies the connection of peripherals and instruments
- **COMPREHENSIVE SOFTWARE**
  Comprises proven software for generating and executing your programs
- **EXTRA CAPABILITY OPTIONS**
  Let you add an extended arithmetic unit, direct memory access, memory parity check, and memory protect
- **REGISTER REFERENCE MICROINSTRUCTIONS**
  Permit the combining of instructions to simplify and speed programming

DESCRIPTION

The combination of powerful software and simple interface make the HP 2116C a good choice for small computer applications. Versatility, expandability, ease of use, reliability, support — these are a few of the things you get when buying a 2116C.

In the 2116C you get a proven general-purpose, 16-bit processor that is built of reliable integrated circuits. Comprehensive standard software enables you to make the most of the 16-bit word length.

A minimum 2116C includes an 8192-word memory, self-contained power supplies, and 16 input/output channels. You can select (or expand to) 16, 24, or 32K all in mainframe. Through the use of optional extenders you can have up to 32 or 48 I/O channels, all of which are a part of the normal I/O addressing and interrupt system.

Besides such options as memory protect, memory parity, and power fail interrupt, there are two important options available with the 2116C. An Extended Arithmetic Unit reduces execution times by providing hardware implementation of such software routines as multiplication and division. Another option, Direct Memory Access, permits I/O data transfer at rates up to 263,000 words per second over any mainframe channel directly to or from memory.

SPECIFICATIONS

MEMORY
Type: Magnetic core
Size: 8192 16-bit words (expandable to 16, 24, or 32K)
Page Size: 1024 words
Direct Addressing: Current page and Base page
Indirect Addressing: All pages
Speed: 1.6 microsecond cycle time
Loader Protection: "Protected" switch disables last 64 locations

ARITHMETIC
Parallel, two's complement binary

COMPUTE SPEED

	Microseconds	With Extended Arithmetic Unit	
Add	3.2	3.2	(1 instruction)
Subtract	4.8	4.8	(2 instructions)
Multiply	112*	19.2	(1 instruction)
Divide	350*	20.8	(1 instruction)
Floating Point Add	487*	302*	
Floating Point Subtract	468*	286*	
Floating Point Multiply	803*	326*	
Floating Point Divide	1590*	350*	

*Subroutine — time approximate

INPUT/OUTPUT
Number of mainframe channels: 16
Total channels with extender: 32 or 48
Channel capacity: 16 bits, parallel transfer
Service Method: priority interrupt hardware, standard
Priority assignment: by position of interface card

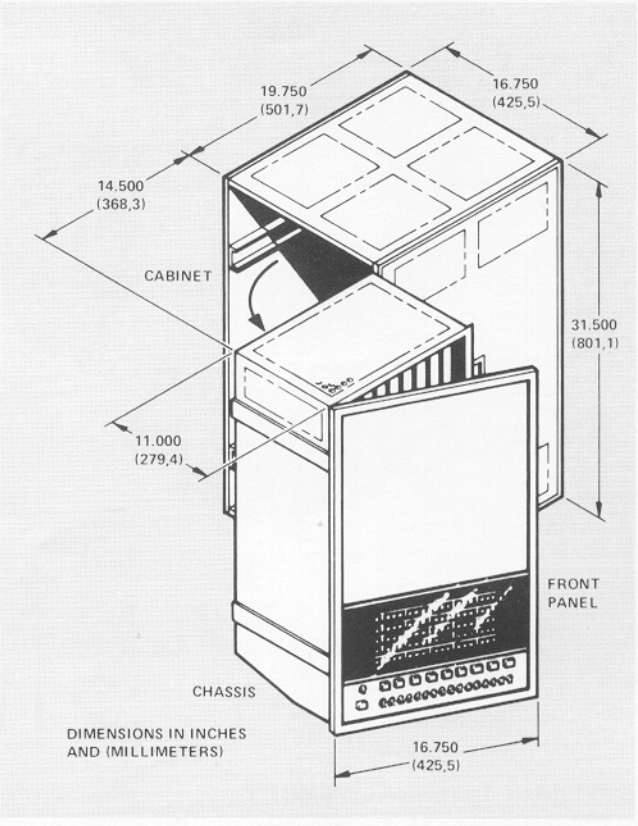
VENTILATION
Intake on sides and back at bottom, exhaust at top. Air flow 600 cfm. Heat dissipation 5500 BTU/hr.

INSTALLATION
For use on table, or mounted in standard 19-inch rack, using adapters furnished (panel height 31-1/2 inches). Requires no special wiring, subflooring, or other special installation preparations.

WEIGHT
Net 230 lb (104 kg)
Shipping 330 lb (150 kg)

POWER REQUIRED
Source: 115/230V ± 10%, 50 to 60 Hz
Consumption: 1000W min to 1600W max, depending on number of I/O interfaces installed.

ENVIRONMENTAL CONDITIONS
From 0° to +55°C (+32° to +131°F)
Relative humidity to 95% at 40°C



OPTIONS
Power Fail: Has highest interrupt priority. Can be used to automatically save register contents and program location if power fails. Optionally halts or resumes execution of the interrupted program when power is restored.

Direct Memory Access: Provides two 16-bit channels, program assignable to any mainframe channel. Maximum transfer rate is 263,000 words per second. Uses one memory cycle per transfer. Block transfers up to 16,384 words.

Parity Check: Verifies parity for all words transferred in or out of memory. Provides front panel indication of error and transfers control to interrupt routine.

Memory Protect: Permits any amount of memory to be "fenced". Inhibits any instruction that attempts to change a protected location and makes address of offending instruction available for software interrogation. Inhibits I/O instructions outside protected area.

Extended Arithmetic Unit: Permits integer multiply, integer divide, double load, double store, long shifts, and long rotations to be performed by hardware rather than program subroutines.

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