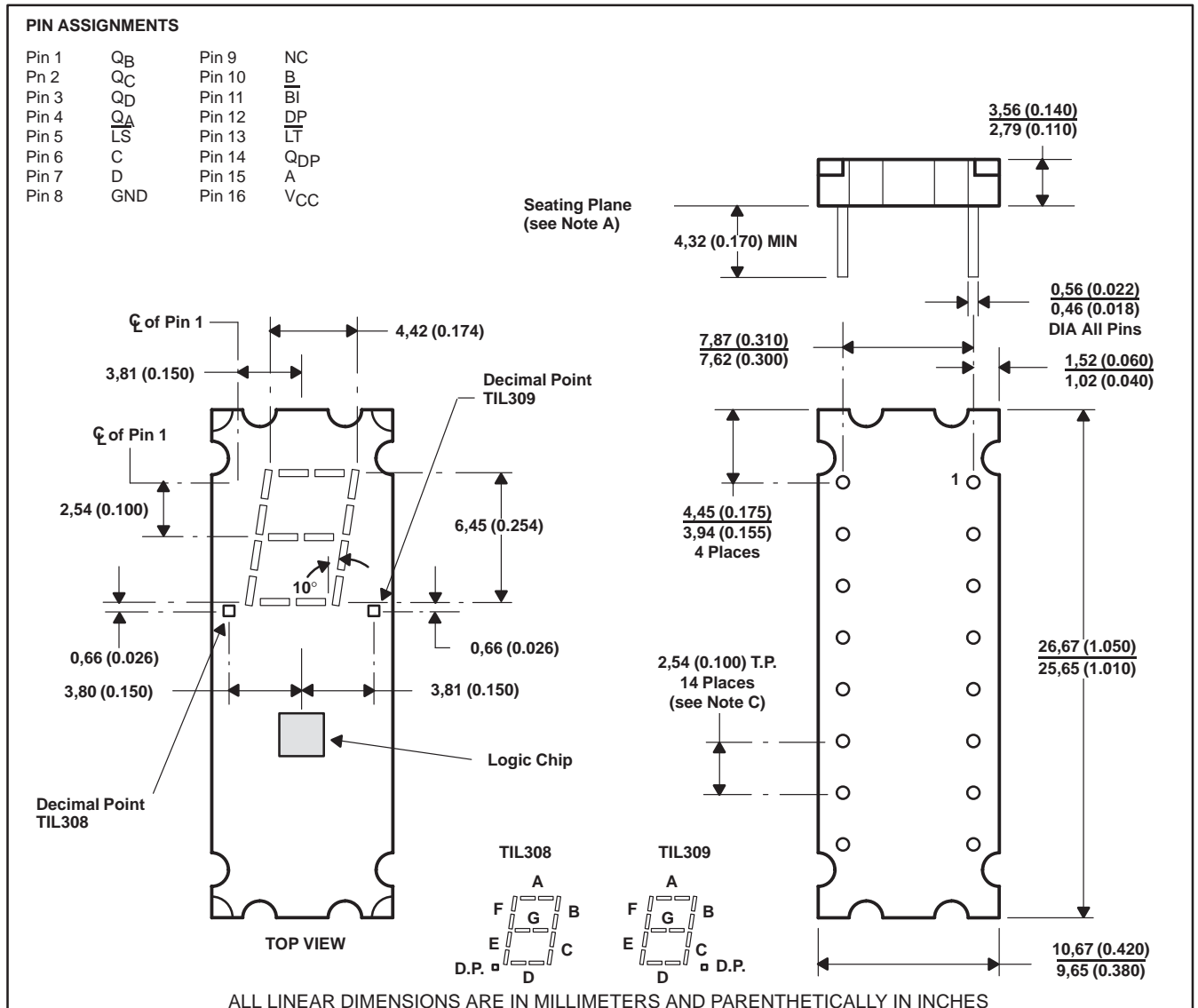


**SOLID-STATE DISPLAYS WITH INTEGRAL TTL MSI CIRCUIT CHIP FOR USE  
 IN ALL SYSTEMS REQUIRING A DISPLAY OF BCD DATA**

- 6,9-mm (0.270-Inch) Character Height
- TIL308 Has Left Decimal
- TIL309 Has Right Decimal
- Easy System Interface
- Wide Viewing Angle
- Internal TTL MSI Chip With Latch, Decoder, and Driver
- Constant-Current Drive for Light-Emitting Diodes

**mechanical data**

These assemblies consist of display chips and a TTL MSI chip mounted on a header with a red molded plastic body. Multiple displays may be mounted on 11,43-mm (0.450-inch) centers.



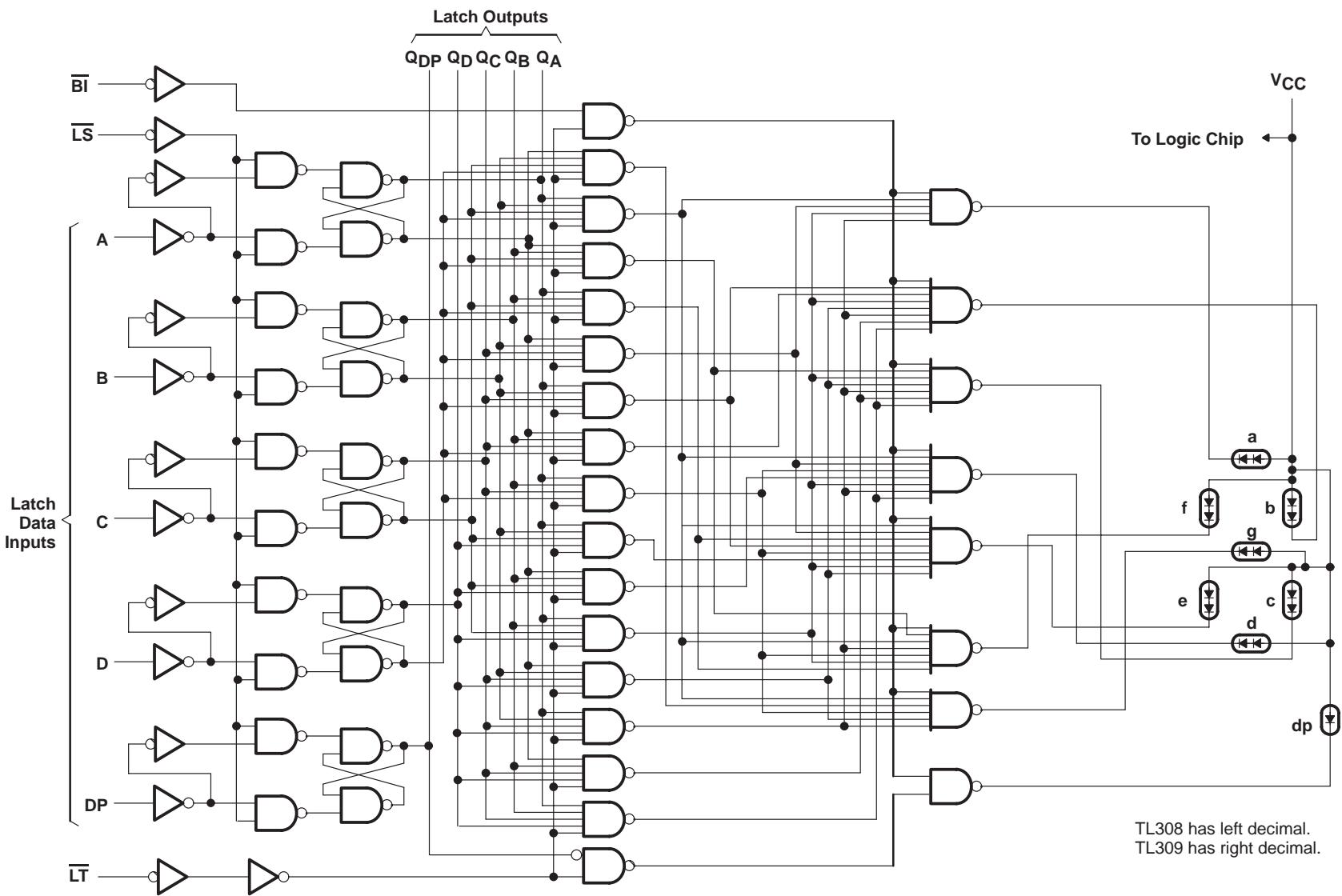
- NOTES: A. Lead dimensions are not controlled above the seating plane.  
 B. Centerlines of character segments and decimal points are shown as dashed lines. Associated dimensions are nominal.  
 C. The true-position pin spacing is 2,54 mm (0.100 inch) between centerlines. Each centerline is located with 0,26 mm (0.010 inch) of its true longitudinal position relative to pins 1 and 16.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



# TIL308, TIL309 NUMERIC DISPLAYS WITH LOGIC

SLBS002-D1096, MARCH 1972-REVISED SEPTEMBER 1992



**description**

These internally-driven seven-segment light-emitting-diode (LED) displays contain a five-bit latch and a decoder/LED driver in a single 16-pin package. A description of the functions of the inputs and outputs of these devices are in the terminal function table.

The TTL MSI circuits contain the equivalent of 78 gates on a single chip. Logic inputs and outputs are completely TTL/DTL compatible. The buffered inputs are implemented with relatively large resistors in series with the bases of the input transistors to lower drive-current requirements to one-half of that required for a standard Series 54/74 TTL input.

Some of the additional features of these displays are as follows:

- Latched BCD and decimal point logic outputs provided to drive logic processors simultaneously with the displayed data
- Minimum number of inputs required . . . 4-line BCD plus decimal point
- Overriding blanking for suppressing entire display or pulse-modulation of LED brightness
- LED test input to simultaneously turn on all display segments and decimal point
- Can be operated in a real-time mode or latched-update-only mode by use of the latch strobe input
- Displays numbers 0 through 9 as well as A, C, E, F, or minus sign
- Can be blanked by entry of BCD 13 or by use of the blanking input
- Decimal point controlled independently with decimal-point latch
- Constant-current-source TTL-LED interface for optimum performance.

The latch outputs except  $Q_{DP}$  are active pullup, and each one, except  $Q_{DP}$ , is capable of driving three standard Series 54/74 loads. The LED driver outputs are designed specifically to maintain a relatively constant on-level current of approximately 7 mA through each LED segment and decimal point. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Power dissipation is typically 575 mW with all segments on.

**Terminal Functions**

PIN		DESCRIPTION
NAME	NO.	
BLANKING Input ( $\overline{BI}$ )	11	When low, will blank (turn off) the entire display. Must be high for normal operation of the display.
Latch Data Inputs A, B, C, D, DP	15, 10, 6, 7, 12	Data on these inputs are entered into the latches under the control of the latch strobe input. The binary weights of the inputs are: A = 1, B = 2, C = 4, D = 8. DP is decimal point latch data input.
Latch Outputs $Q_A$ , $Q_B$ , $Q_C$ , $Q_D$ , $Q_{DP}$	4, 1, 2, 3, 14	The BCD data that drives the decoder is stored in the five latches and is available at these outputs. The binary weights of the outputs are: $Q_A = 1$ , $Q_B = 2$ , $Q_C = 4$ , $Q_D = 8$ . $Q_{DP}$ is decimal point latch output.
LATCH STROBE Input ( $\overline{LS}$ )	5	When low, the data in latches follow the data on the latch inputs. When high, the data in the latches are held constant and are unaffected by new data on the latch inputs.
LED TEST Input ( $\overline{LT}$ )	13	When low, will turn on the entire display, overriding the data in the latches and the blanking input. Must be high for normal operation of the display.

# TIL308, TIL309 NUMERIC DISPLAYS WITH LOGIC

SLBS002-D1096, MARCH 1972-REVISED SEPTEMBER 1992

FUNCTION TABLE

FUNCTION	LATCH INPUTS						BLANKING INPUT	LED TEST	LATCH OUTPUTS					DISPLAY	
	D	C	B	A	DP	STROBE			Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>	Q <sub>DP</sub>	TIL308	TIL309
0	L	L	L	L	L	L	H	H	L	L	L	L	L	0	0
1	L	L	L	H	H	L	H	H	L	L	L	H	H	.1	1
2	L	L	H	L	L	L	H	H	L	L	H	L	L	2	2
3	L	L	H	H	H	L	H	H	L	L	H	H	H	.3	3
4	L	H	L	L	L	L	H	H	L	H	L	L	L	4	4
5	L	H	L	H	H	L	H	H	L	H	L	H	H	.5	5
6	L	H	H	L	L	L	H	H	L	H	H	L	L	6	6
7	L	H	H	H	H	L	H	H	L	H	H	H	H	.7	7
8	H	L	L	L	L	L	H	H	H	L	L	L	L	8	8
9	H	L	L	H	H	L	H	H	H	L	L	H	H	.9	9
A	H	L	H	L	L	L	H	H	H	L	H	L	L	A	A
Minus Sign	H	L	H	H	H	L	H	H	H	L	H	H	H	.-	.-
C	H	H	L	L	L	L	H	H	H	H	L	L	L	C	C
Blank	H	H	L	H	H	L	H	H	H	H	L	H	H	.	.
E	H	H	H	L	L	L	H	H	H	H	H	L	L	E	E
F	H	H	H	H	H	L	H	H	H	H	H	H	H	.F	F.
Blank	X	X	X	X	X	X	L	H	X	X	X	X	X		
LED TEST ( $\overline{\text{LT}}$ )	X	X	X	X	X	X	X	L	X	X	X	X	X	.B	B.

H = high level, L = low level, X = irrelevant.

DP input has arbitrarily been shown activated (high) on every other line of the table.

## absolute maximum ratings over operating case temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1): Continuous	5.5 V
Nonrepetitive peak, $t_w \leq 100$ ms	7 V
Input voltage (see Note 1)	5.5 V
Operating case temperature range, $T_C$ (see Note 2)	0°C to 85°C
Storage temperature range	-25°C to 85°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. Case temperature is the surface temperature of the plastic measured directly over the integrated circuit. Forced-air cooling may be required to maintain this temperature.

## recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
Normalized fanout from each output, N (to Series 54/74 integrated circuits)	Low logic level	Q <sub>DP</sub>		1	
		Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub>		3	
	High logic level	Q <sub>DP</sub>		3	
		Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub>		6	
Latch strobe pulse duration, $t_w$		45			ns
Setup time, $t_{su}$	Latch data input (DP) before latch strobe ( $\overline{\text{LS}}$ ) $\uparrow$	60			ns
Hold time, $t_h$	Latch data input (DP) after latch strobe ( $\overline{\text{LS}}$ ) $\uparrow$	0			ns
Operating case temperature, $T_C$		0		70	°C



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electrical characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
V <sub>IH</sub>	High-level input voltage		2			V	
V <sub>IL</sub>	Low-level input voltage				0.8	V	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.75 V, I <sub>I</sub> = -12 mA			-1.5	V	
V <sub>OH</sub>	High-level output voltage	Q <sub>DP</sub>	V <sub>CC</sub> = 4.75 V, I <sub>OH</sub> = -120 μA	2.4		V	
		Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub>	V <sub>CC</sub> = 4.75 V, I <sub>OH</sub> = -240 μA				
V <sub>OL</sub>	Low-level output voltage (see Note 3)	Q <sub>DP</sub>	V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 1.6 mA		0.4	V	
		Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub>	V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 4.8 mA				
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 5.5 V			1	mA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 2.4 V			20	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0.4 V			-0.8	mA	
I <sub>OS</sub>	Short-circuit output current	Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub>	V <sub>CC</sub> = 5.25 V		-9	-27.5	mA
		Q <sub>DP</sub>			-1	-3.2	
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = 5.25 V, All inputs at 0 V		115	180	mA	
I <sub>v</sub>	Luminous intensity (see Note 4)	Figure B	V <sub>CC</sub> = 5 V		700	1200	μcd
		DP Input			40	70	
λ <sub>p</sub>	Wavelength at peak emission	V <sub>CC</sub> = 5 V, See Note 5			660	nm	
Δλ	Spectral bandwidth	V <sub>CC</sub> = 5 V, See Note 5			20	nm	

† All typical values are at V<sub>CC</sub> = 5 V.

NOTES: 3. This parameter is measured with the display blanked.

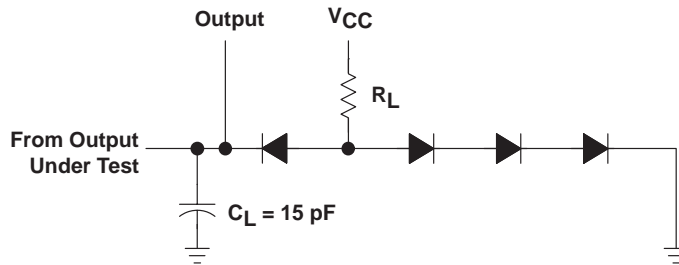
4. Luminous intensity is measured with a light sensor and filter combination that approximates the CIE (International Commission on Illumination) eye-response curve.

5. These parameters are measured with all LED segments and the decimal point on.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>C</sub> = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A, B, C, D, DP	Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub> , Q <sub>DP</sub>	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1.2 kΩ, See Figure 1		35		ns
t <sub>PHL</sub>					40		

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

B. All diodes are 1N3064.

C. Measurements made with  $\overline{\text{LS}}$  input grounded.

Figure 1. Load Circuit

TYPICAL CHARACTERISTICS

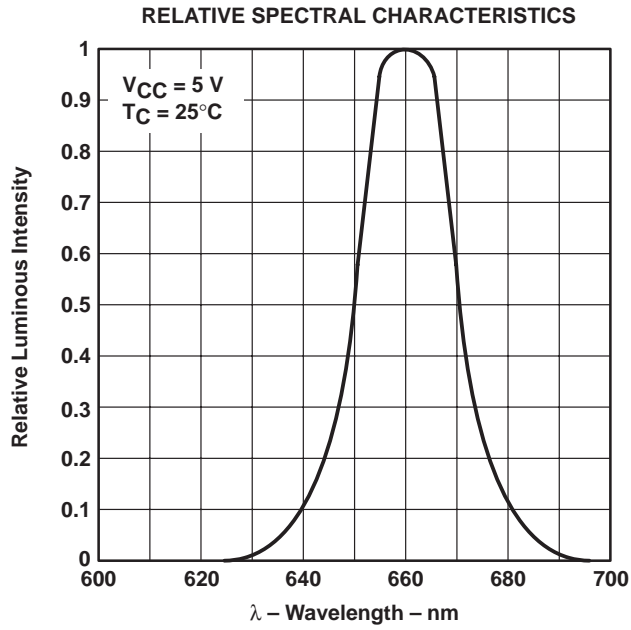


Figure 2

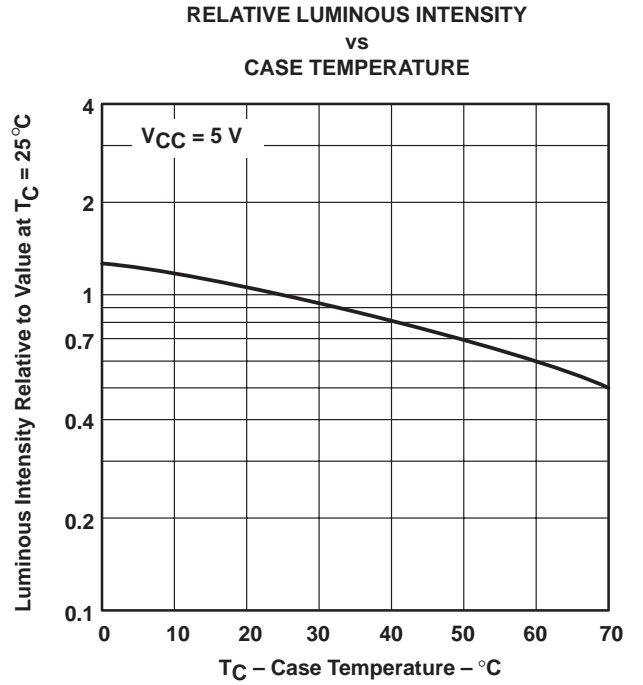


Figure 3

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TIL308	OBSOLETE			16		TBD	Call TI	Call TI
TIL309	OBSOLETE			16		TBD	Call TI	Call TI
TIL309	OBSOLETE			16		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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