SOLUTIONS

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INTEL BRINGS HARMONY TO THE FACTORY FLOOR

Megabits to Megabytes: Bubble Memory System Design and Board Layout

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The sophisticated seven-component bubble memory selection from Intel represents the most integrated solution for reliable, non-volatile memory applications. Bubble memory's solid-state operation can offer much higher system reliability than that obtainable with other mass storage technologies such as standard tape and disk drives, both of which can suffer due to shock and vibration. Bubble memory is compact, requires no routine maintenance, and can operate in extreme temperatures, making it ideal for applications such as industrial control or military systems that require consistent and maintenance-free operation. Intel's Bubble Memory Controller (BMC) also makes interfacing to any microprocessor or microcontroller easy.

Component bubble memory designs present no form factor limitations, allowing the system designer freedom to build a mass storage system to custom specifications. For the most part, a bubble memory system is designed and assembled much like any other component design. However, there are a few unique considerations to be aware of before designing any bubble memory system. The attention paid to a few simple design guidelines will ensure the system design engineer a successful bubble memory system.

System Overview

The Intel bubble memory solution consists of a highly sophisticated Bubble Memory Controller (BMC) that can support up to an entire megabyte for the 7200 controller, or up to four megabytes using the new 7225 Four-Megabit Bubble Memory Controller. In other words, one controller can support up to eight Bubble Storage Units (BSUs).

Bubble Memory Controller (BMC)

The Bubble Memory Controller is a VLSI chip that provides a complete bi-directional interface between the host microprocessor system and the Bubble Memory Storage Unit (BSU). The bubble memory designer's primary task is to interface the Bubble Memory Controller (BMC) to the host microprocessor system. The interface to the BMC is much like that of any standard peripheral controller, such as a floppy-disk controller or a DMA controller. The actual electrical interface between the BMC and the BSU is provided by Intel, since this part of the system will remain entirely unchanged from one design to another. Because the BMC is a peripheral controller, it also requires a certain amount of software for complete operation. Generally, this code has an approximate length of 1K-bytes. Upon receipt of a software command from the host processor, the BMC generates the proper timing and control signals necessary to operate the remaining support circuitry in each BSU.

The functional description of each of the six support components found in a Bubble Storage Unit (BSU) is as follows (See figure 1):

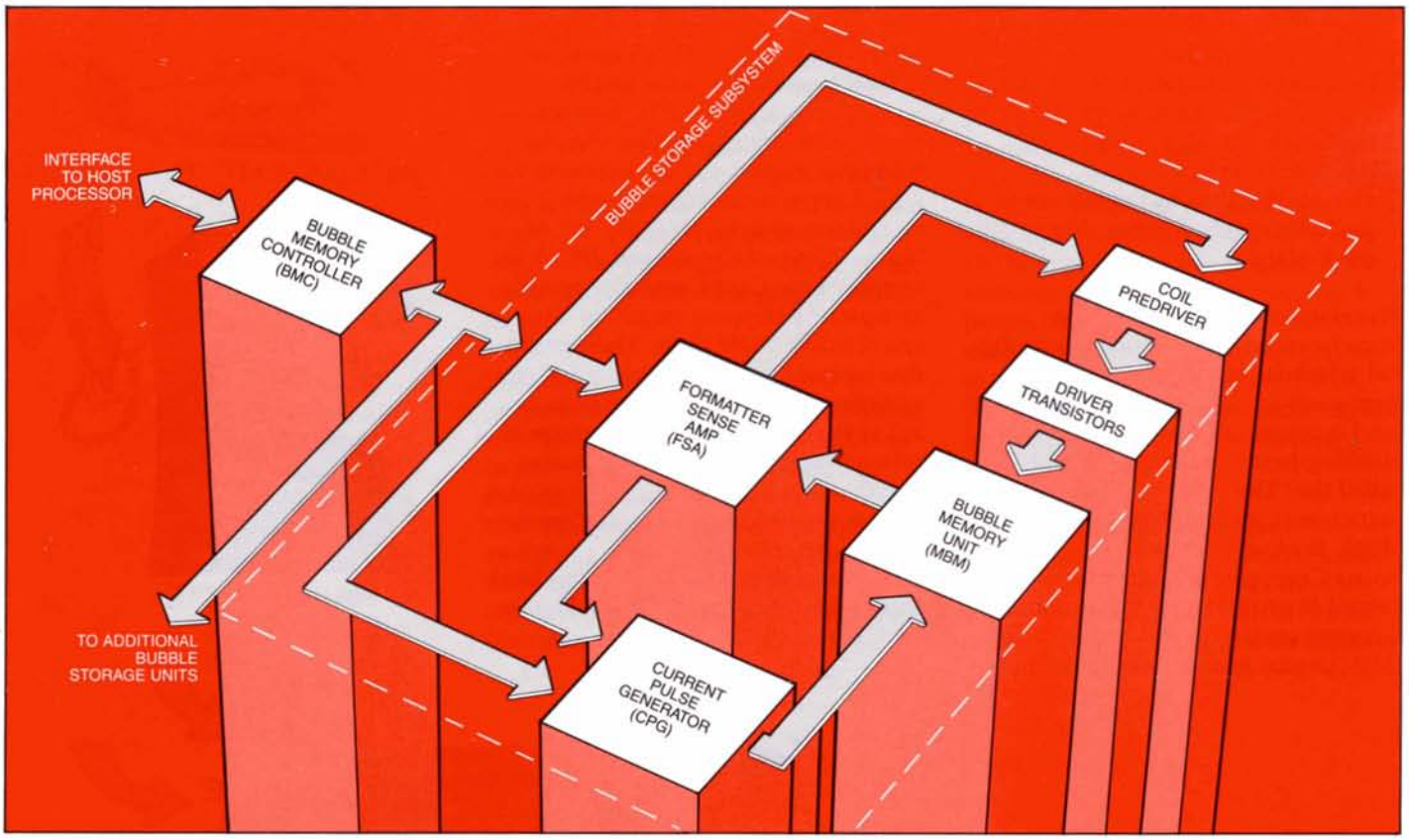

Figure 1: A complete bubble memory storage system

Magnetic Bubble Memory (MBM)
One Megabit Density: 7110A, 7110AZ
Four Megabit Density: 7114

The Magnetic Bubble Memory (MBM) is a high-density, highly reliable, non-volatile solid state memory based on magnetic bubble technology. It is contained in a 20-pin leaded package surrounded by a mu-metal magnetic shield. Intel offers both one megabit and four megabit bubble memories. The solid-state operation of bubble memory makes it immune to the failures common to other forms of mass storage such as tape and disk. Bubble memory is stock and vibration-resistant, immune to airborne particles, and operates over a wide temperature range. Its magnetic technology guarantees non-volatile data integrity without the need for batteries. Furthermore, it has unlimited read/write capabilities when compared to other solid-state memory technologies such as EPROMs and E²PROMs. Data within the bubble memory device is organized serially. However, to aid in standard system design, the bubble memory controller assimilates the bit-wide data stream from a bubble memory and converts it to a byte-wide data path for the host processor.

Current Pulse Generator (CPG)
One Megabit Density: 7230
Four Megabit Density: 7234

The Current Pulse Generator (sometimes called a function generator) generates the necessary precision current waveforms to input and output data from the MBM.

Formatter Sense Amplifier (FSA)
One Megabit Density: 7242
Four Megabit Density: 7245

The Formatter/Sense Amplifier (FSA) interfaces directly with both the MBM and the BMC. It converts the low level signals from the bubble memory detector outputs into TTL-level logic signals. The FSA also enables the generation of magnetic bubbles within the MBM. The FSA performs the additional tasks of data formatting, error correcting, and mapping the redundancy built into the MBM (redundancy is built into many high-density memory devices to increase manufacturing yields).

Coil Pre-Driver (CPD)

The 7250 is used in both one megabit and four megabit systems. The data within a bubble memory is moved and accessed by passing currents of the proper magnitude and phase through two coils within the MBM. The Coil Pre-Driver (CPD) works in conjunction with the BMC to generate the signals for driving the X and Y coil drive transistors of the bubble memory.

Drive Transistors
One Megabit Density: (2) 7254
Four Megabit Density:(4) 7254

There are two sets of drive transistors in a bubble memory system. One set drives the X coil inside the MBM while the other drives the Y coil. Both act as analog switches to produce the high current coil driver waveforms. The high current waveforms create a rotating magnetic field as they pass through the internal coils of the MBM.

Board Layout: How to Avoid the Pitfalls

Once the design engineer has completed the simple task of interfacing the BMC to the host microprocessor or microcontroller, the next aspect of design is the board layout. The most critical layout area on a bubble memory board exists around the traces between the bubble memory detector output and the inputs to the FSA. These signals — which are on the order of only five millivolts in amplitude for the 7110A and thirty millivolts for the 7114—must be protected from noise. The detector lines carry the low level data signals to the FSA, where the binary state is resolved and then converted to TTL-level signals, as shown in Figure 2. Reducing spurious noise on the detector traces improves bubble detection and increases system performance.

Though it may appear difficult to isolate the low level detector signals from the high current switching transients generated by the coil drivers, there are some simple design rules to follow to ensure reliable operation.

First, the connections between the bubble detector outputs and the FSA inputs should be kept as short and direct as possible. This applies to the path through the signal filter as well (which is provided in the system schematic). Otherwise, long signal traces can act as "antennae" to receive induced noise from higher-level signals. A decreased path length prevents any significant signal loss. The effect of noise is also reduced through the actual design of the bubble detection mechanism using differential pair outputs to the FSA. Since the output is a differential pair, these signal traces should have approximately the same conductor length so that both sides of the signal path have balanced resistances.

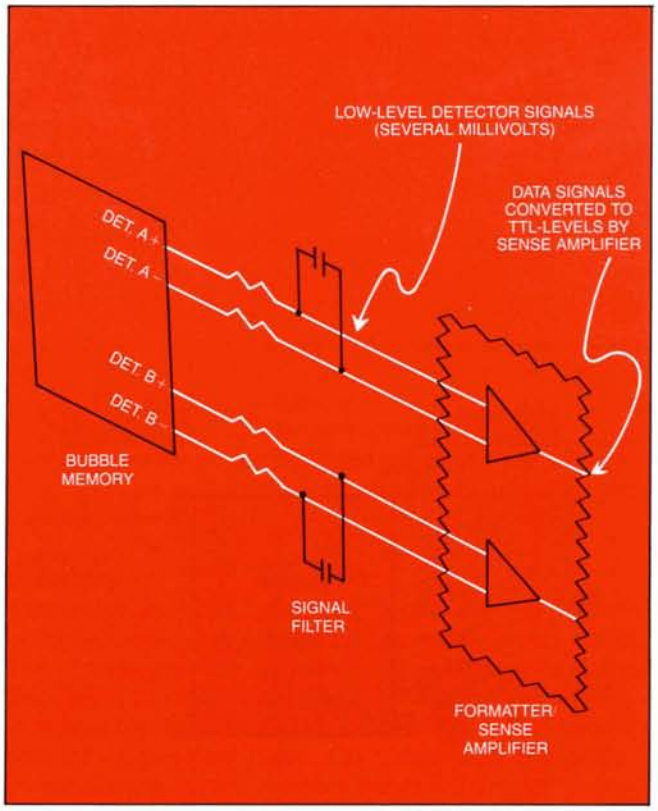

Figure 2: Signal to TTL-level conversion

Second, it is imperative that no digital logic signals cross or come within close proximity to the detector traces. The circuit board designer should avoid running digital logic signals parallel to the detector traces. A separation of at least 0.5 inches is sufficient. Even in multilayer designs, logic traces should not run below the detector traces; the detector lines are only several millivolts in amplitude. A high speed logic line can easily cause noise-induced data errors through bad layout.

Third, the X and Y coil drive input traces to the MBM should be separated from the detector signals by as much as possible. The coil drive signals carry large currents and are switched at 50KHz frequencies. The switching transients can induce noise unless the coil drive signals are routed correctly; by separating these signals from the detector output signals, the circuit board designer can decrease the amount of noise induced onto the detector outputs.

The X and Y coil drive input traces from the 7254 drive transistor sets to the X and Y coils contained within the MBM should also be kept as short as possible. Placing the driver transistors in close proximity to the MBM near its coil input pins is the best method. In addition, since the coil drive signals carry large currents, they should also have larger conductor line widths of at least 0.1 to 0.2 inches. Lastly, by having the coil drive signals form a loop of minimum enclosed area, the transmitted noise is further reduced. An example of a good layout for the X and Y coil drive signals is shown in Figure 3.

The majority of noise problems can be solved by electrically isolating the small detector output signals from the rest of the system. Reducing spurious noise on the detector traces improves bubble detection and increases system performance. This is accomplished by providing sufficient grounding around the detector traces. To implement a ground plane between the MBM and the FSA, the circuit board designer can use a variety of techniques. Two methods are presented here—a two-layer and a multi-layer technique.

A multi-layer circuit board is suggested for most bubble memory board designs since it represents a more reliable design method than a two-layer circuit board. However, a two-layer board is quite appropriate for single-bubble systems, since this will typically have a less complicated layout than a multi-bubble system and is sometimes cost sensitive.

When using a two-layer circuit board, one layer should be dedicated to routing the detector lines in a surrounding ground plane while the second layer should be dedicated to a local ground plane under the detector signals. Therefore, not only does the ground plane physically isolate the detector signals from the other board signals, but it isolates them electrically as well. This is shown in Figure 4.

The ideal four-layer circuit board uses quite a different approach. By routing the detector traces in a ground plane surrounded above and below by other ground planes, a "pseudo-coaxial" shield is formed around the low-level signals from the MBM, as shown in Figure 5. However, in some designs this method may become too space- and layout-intensive to use on a multi-layer board. In these cases, one of the ground planes can be substituted with one of the DC power planes. This works because the DC power plane acts as an AC grounding plane if the power supply has sufficient capacity.

Some precautionary notes about the ground plane solution are in order, regardless of how many layers are used in the circuit board. A designer must be careful to prevent other components which are not part of the bubble detection mechanism (i.e., parts other than the MBM or the FSA) from occupying the same branch of the localized ground planes. Again, it is important that the low level signals from the bubble detectors do not share a ground branch with high-level components such as the coil pre-driver or the current pulse generator. Noise can be induced across the detector traces if a ground return path from a noisy component flows through the local detector ground shield.

Power and Power-Fail Considerations

After completing the bubble memory board layout, the next most important design aspect is the power system. A power-fail (or power-down data protection) circuit is required by all non-volatile memories that are written in-circuit. This includes both solid state as well as rotating media like E^2PROMs, floppy disks, tape drives, etc. A power-fail circuit

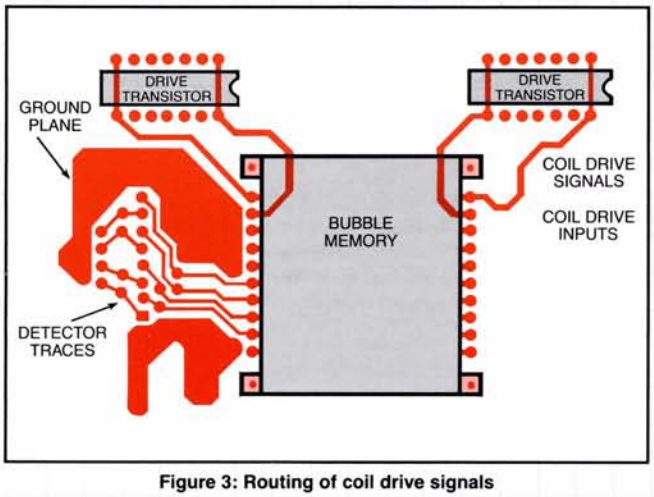

Figure 3: Routing of coil drive signals

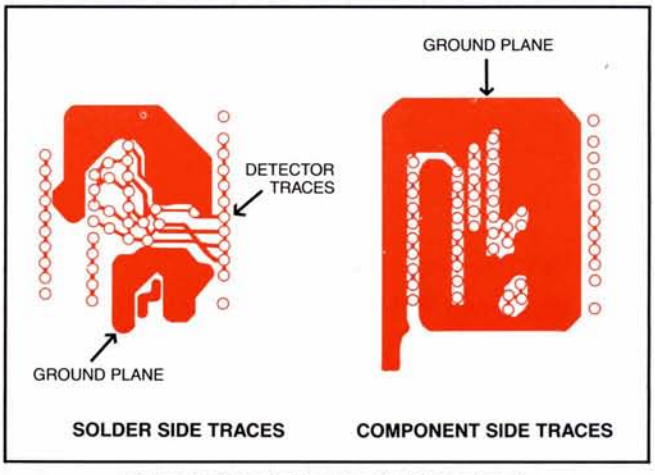

Figure 4: Ground plane for a two-layer board

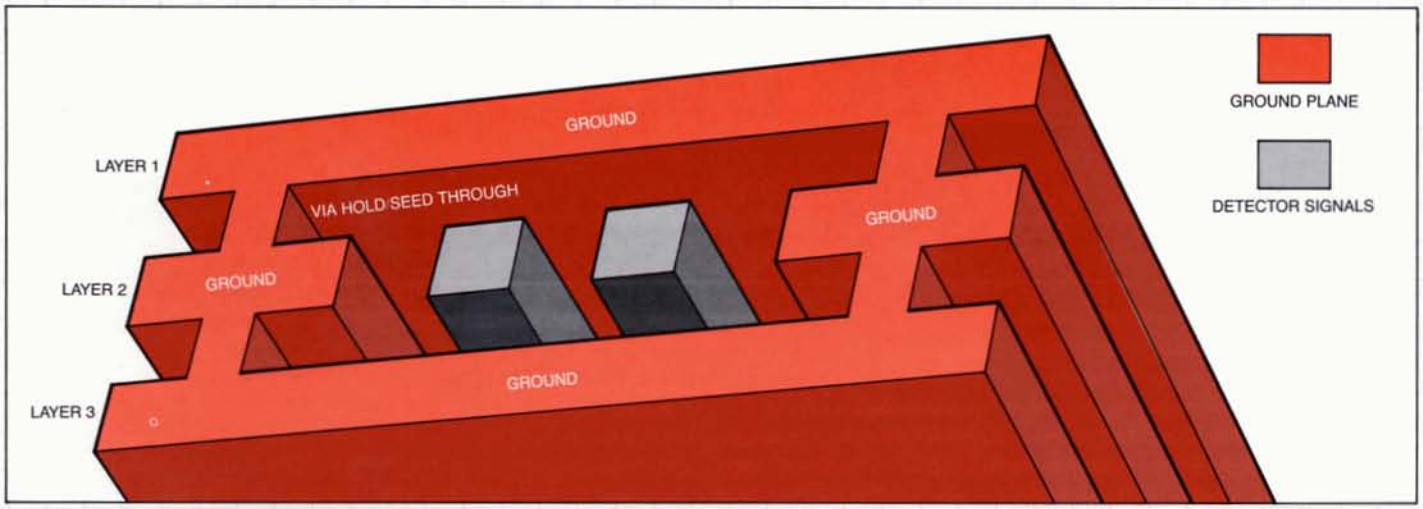

Figure 5: Cross-section of "pseudo" coaxial shielding

safeguards the data stored in the non-volatile memory from the ambiguous conditions that exist on power-up and power-down (spurious writes, for example). In a bubble memory system, the power-fail circuitry performs the additional task of ensuring that all of the system housekeeping is completed before the system powers down. It also guarantees that no extraneous data is written into the bubble before the support components are ready during a power-up sequence; otherwise, it is possible to "scramble" the MBM's data.

Intel's bubble memory system requires only two DC operating voltages: +5V and +12V. To allow the power-fail circuit time to complete its task, the maximum power decay rate of the bubble memory system power supply is specified, as shown below.

- ☐ +12V supply (V_{DD}) voltage tolerance of (+/−)5%, with a power-off/power-fail decay rate of no more than 1.1 V/ms.
- ☐ +5V supply (V_{CC}) voltage tolerance of (+/−)5%, with a CC power-off/power-fail decay rate of no more than 0.45 V/ms.

The maximum power decay rate is specified so that the support components can shut down the system in an orderly fashion once an imminent power-fail condition is detected. If the power decays too quickly, the silicon support circuits will not have enough power to perform the shutdown procedure correctly. The power-fail circuitry depends on the internal capacitance of the power supply to provide the necessary power. Most power supplies have enough internal capacitance to meet the power decay rate specification. Strict adherence to these specifications will prevent any "scrambling" of the data stored in the bubble memory.

Another method to indicate power loss is through the power supply itself. Many modern power supplies have the capability of providing a TTL level signal that indicates an imminent AC power loss. This capability can be utilized in conjunction with the power-fail circuitry to give the system warning of a power-down.

One point to consider is the effect of an over voltage protection circuit (OVP) — also called a crowbar — on the power decay specification. In a crowbarred supply, an SCR is triggered by an overvoltage. The SCR then pulls the system power supply to some much lower voltage (near ground) almost instantaneously to prevent overvoltage-induced component damage. If triggered, the crowbar can violate the power decay spec and lead to potential data loss. Therefore, crowbarring must be either eliminated or prevented until the bubble memory system has completed an orderly shutdown through the power-fail circuitry. Since a majority of crowbar conditions are caused by noise and voltage spikes on the AC power line, adding line filtering to the AC line will eliminate a majority of crowbarring.

Another important aspect when designing the power system is using power capacitors placed around each of the drive transistors and each MBM. These act as a current storage reservoir from which the drive coils can absorb and dump current. Without these capacitors, the inherent board inductance and resistance can cause a voltage drop and a subsequent power-fail condition, as well as variations in the coil drive amplitudes.

The power capacitors actually perform another function. The drive coils require an almost linear current ramp to drive the rotating magnetic field in the correct manner. Even with the small amount of inductance and resistance in the board, the linear current ramp will take on the form of an LR current curve—thus driving the field incorrectly. By placing the capacitors directly around the MBM coil driver, the amount of undetermined inductance and resistance from the circuit board is minimized.

Summary

The design and layout of an Intel bubble memory system is no more complicated than that of any other memory system. The sophisticated bubble memory support components ease the design process considerably. The prime consideration in bubble memory board layout is to decrease all potential sources of electrical noise. Once designed and properly constructed, a bubble memory board will provide years of maintenance-free operation. ☐