



7230 CURRENT PULSE GENERATOR FOR BUBBLE MEMORIES

7230	0 to 70°C
7230-4	10 to 55°C
7230-5	-20 to +85°C

- TTL Compatible Inputs
- Provides All Pulses for Intel Bubble Memories
 - Replicate, Swap, Generate, Boot Replicate and Bootswap
- Current Sink Outputs Designed to Directly Drive Bubble Memory
- Direct Interface to Bubble Memory Controller
- Automatic Power Fail and Reset
- Operates from +5 and +12 Volts Only
- Schottky Bipolar Technology
- Standard 22-Pin Dual-In-Line Package

The Intel 7230 is a Current Pulse Generator (CPG) designed to drive Intel Magnetics Bubble Memories. The 7230 is a Schottky Bipolar, TTL input compatible device that converts digital timing signals to analog current pulses. The CPG provides all pulses for Intel Magnetics Bubble Memories (7110 Family). These include Replicate, Swap, Generate, Boot Replicate and Bootswap pulses. The high-current sinking outputs directly drive the bubble memory. It also directly interfaces to the Intel Magnetics Bubble Memory Controller (7220-1) and Formatter/Sense amplifier (7242).

The 7230 operates from 5-volt and 12-volt power supplies and is in a standard 22-pin dual-in-line package.

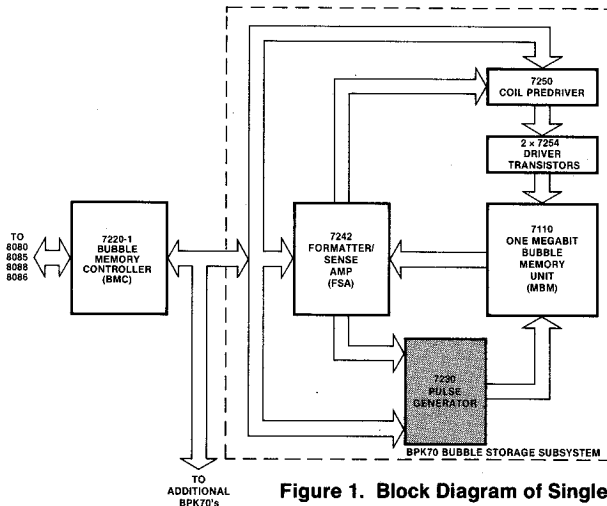


Figure 1. Block Diagram of Single Bubble Memory System—128K Bytes

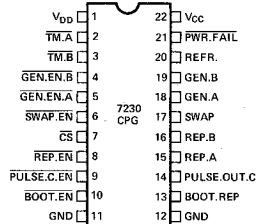


Figure 2. Pin Configuration

EXTERNAL RESISTOR REQUIREMENTS

Connect a 1% 3.48K ohm resistor based between pin 20 and ground or referenced current switch as outlined in BPK72 User's Manual.

Table 1. Pin Description

Symbol	Pin No.	Description
BOOT.EN	10	An active low input enabling the BOOT.REP output current pulse.
BOOT.REP	13	An output providing the current pulse for bootstrap loop replication in the bubble memory.
BOOT.SWAP	14	An output providing a current pulse which may be used for writing data into the bootstrap loop.
BOOT.SWEN	9	An active low input enabling the BOOT.SWAP output current pulse.
CS	7	An active low input for selecting the chip. The chip powers down during deselect.
GEN.A	18	An output providing the current pulse for writing data into the "A" quads of the bubble memory.
GEN.B	19	An output providing the current pulse for writing data into the "B" quads of the bubble memory.
GEN.EN.A	5	An active low input enabling the GEN.A output current pulse.
GEN.EN.B	4	An active low input enabling the GEN.B output current pulse.
PWR.FAIL	21	An active low, open collector output indicating that either V_{CC} or V_{DD} is below its threshold value.
REFR.	20	The pin for the reference current generator to which an external resistance must be connected.
REPA	15	An output providing the current pulse for replication of data in the "A" quads of the bubble memory.
REPB	16	An output providing the current pulse for replication of data in the "B" quads of the bubble memory.
REPEN	8	An active low input enabling the REPA and REPB outputs.
SWAP	17	An output providing the current pulse for exchanging the data between the input track and the storage loops in the bubble memory.
SWAPEN	6	An active low input enabling the SWAP output.
TM.A	2	An active low timing signal determining the cut pulse widths of the BOOT.REP, GEN.A, GEN.B, REPA and REPB outputs.
TM.B	3	An active low timing signal determining the transfer pulse widths of the BOOT.REP, GEN.A, GEN.B, REPA and REPB outputs.

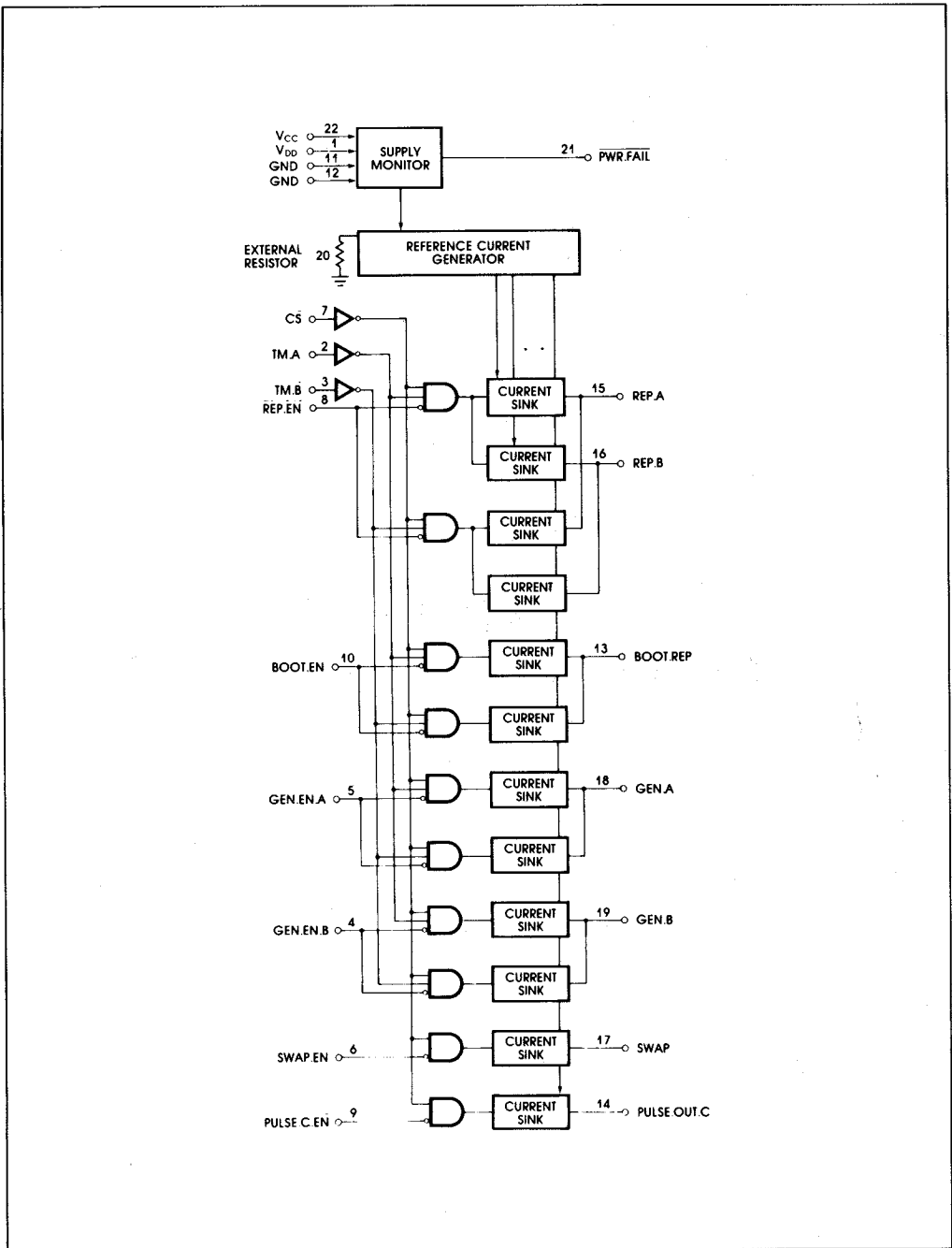


Figure 3. Logic Diagram

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-40° to +100°C
Storage Temperature	-65°C to +150°C
V _{CC} and Input Voltages	-0.5V to +7V
V _{DD} and Output Voltages	-0.5V to +12.6V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = range specified in Table 1; V_{CC} = 5.0V ± 5%, ±5% V_{DD} = 12V ± 5%; unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I _{IL}	Input Low Current			-0.4	mA	V _{IL} = 0.4V, V _{CC} = 5.25V
I _{IH}	Input High Current			20	μA	V _{IH} = V _{CC} = 5.25V
V _{IL}	Input Low Voltage			0.8	V	
V _{IH}	Input High Voltage	2.0			V	
V _C	Input Clamp Voltage			-1.5	V	I = -18 mA, V _{CC} = 4.75V
I _{CEX1}	Output Leakage Current (All Outputs except PWR.FAIL)			1.0	mA	V _{CC} = 5.25V, V _{DD} = 12.6V
I _{CEX2}	PWR.FAIL Output Leakage Current			40	μA	V _{OH} = V _{CC} = 5.25V
V _{OL}	PWR.FAIL Output Low Voltage			0.4	V	I _{OL} = 4 mA, V _{CC} = 4.75V
I _{CC1}	Current from V _{CC} —Selected		30	45	mA	CS = V _{IL} , V _{CC} = 5.25V
I _{DD1}	Current from V _{DD} —Selected		20	35	mA	CS = V _{IL} , V _{CC} = 5.25V
I _{DD2}	Current from V _{DD} —Power Down		12	19	mA	CS = V _{IH} , V _{DD} = 12.6V

A.C. CHARACTERISTICS* V_{CC} = 5V ± 5%; V_{DD} = 12V ± 5%

Symbol	Parameter	Min.	Max.	Unit
t _{ENON}	Delay On		260	ns
t _{DISOFF}	Delay Off		70	ns
t _{CSON}	CS Enable		500	ns
t _{CSOFF}	CS Disable		70	ns

*These parameters are sample tested, not 100% tested.

POWER FAIL CHARACTERISTICS** T_A = 0°C to 70°C

	Min.	Typ.	Max.	Test Conditions
V _{CC} TH	4.43V	4.60V	4.70V	
V _{DD} TH	10.75V	11.10V	11.28V	

**Power fail characteristics apply to 7110 Bubble Memory Data Integrity only and not to full memory operation.

CAPACITANCE* ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions*
C_{IN}	Input Capacitance		10	pF	

*This parameter is periodically sampled and not 100% tested. Condition of measurement is $f = 1\text{ MHz}$.

OUTPUT CURRENTS ($T_A =$ range specified in Table 1, $V_{CC} = 5.0\text{V} \pm 5\%$, $V_{DD} = 12\text{V} \pm 5\%$)

Parameter	Current (mA)			Test Conditions			
				Voltage Out		Voltage Out (7230-5 only)	
	Min.	Nom.	Max.	Min.	Max.	Min.	Max.
GEN.A, GEN.B CUT	62	75	81	5.7	11.5	5.5	11.6
GEN.A, GEN.B TRANSFER	34	40	49	5.7	12.2	5.5	12.2
REPA, REPB CUT	170	200	240	3.7	9.0	3.4	9.3
REPA, REPB TRANSFER	126	145	160	3.7	11.2	3.4	11.4
SWAP	111	125	134	3.1	9.7	2.7	9.9
BOOT.REP CUT	85	100	110	7.8	12.0	7.7	12.1
BOOT.REP TRANSFER	63	75	80	7.8	12.4	7.7	12.4
BOOT.SWAP	63	75	80	9.1	12.2	9.0	12.3

TWO-LEVEL PULSES ARE DEFINED AS SHOWN:

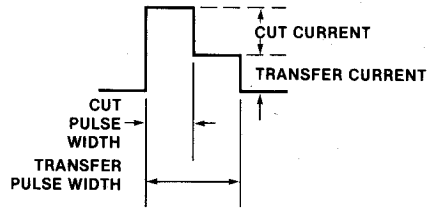
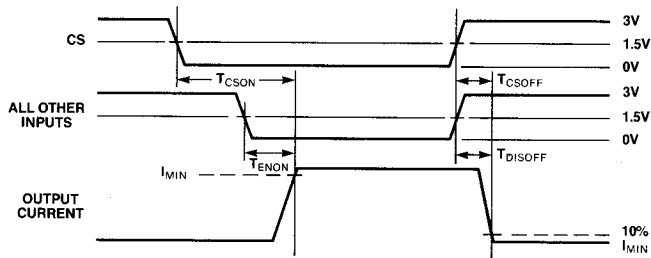


Figure 4. Output Pulse Diagram

WAVEFORM





INTEL CORPORATION, 3065 Bowers Avenue, Santa Clara, CA 95051 (408) 987-8080